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Secondary Side CMOS Feedback Control Integrated Circuit

by

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B.S. Electrical Engineering, United States Air Force Academy

(1988)

Submitted in Partial Fulfillment
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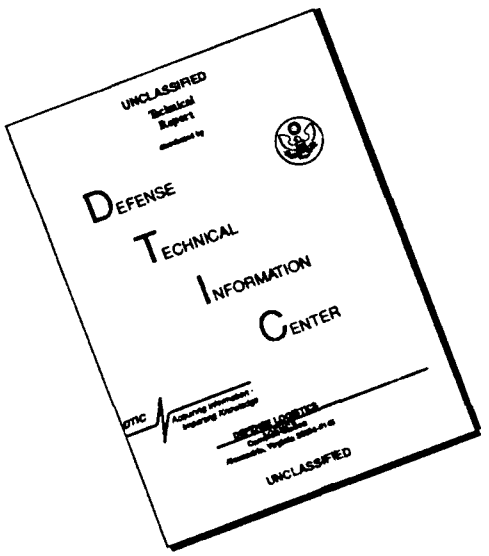

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Secondary Side CMOS Feedback Control Integrated Circuit

by

William P. Wilkinson

Submitted to the

Department of Electrical Engineering and Computer Science

on May 11, 1990 in partial fulfillment of the requirements

for the Degree of Master of Science.

Abstract

This thesis describes the development of a CMOS secondary side feedback control integrated circuit for a power converter. The feedback controller was designed for use in miniaturized point-of-load DC-DC switching power converters. The integrated circuit compares the output of the converter to an on-chip reference voltage and encodes the resulting error signal on an amplitude modulated carrier square wave.

The circuit was designed and verified with extensive computer simulations before being fabricated through the MOSIS program in the 2μ, nwell CMOS process. Errors in the integrated circuit layout were repaired using a Focused Ion Beam, demonstrating the beam's ability to make both connections and detachments on integrated circuits.

The design included four major subcells, a temperature independent bandgap voltage reference, an error amplifier, an oscillator, and an amplitude modulator. Subcell testing demonstrated the suitability and versatility of CMOS for high-density power converter control circuitry.

Thesis Supervisor: Professor Martin F. Schlecht

Title: Associate Professor of Electrical Engineering and Computer Science

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

In recent years, VLSI microprocessing techniques have greatly reduced the size of computer logic circuits, resulting in faster, smaller computers. However, power conversion technology has not kept pace with electronic circuit miniaturization. Computer power supplies continue to adhere to a centralized architecture and a low voltage distribution system. Consequently, the power supply and distribution system now occupy as much as one-third of the computer's total volume.

Currently, researchers at MIT are developing smaller power supplies that would be located directly on the computer logic boards [1]. The point-of-load conversion architecture shown in Fig. 1.1 would replace the single, large power supply used in computers today. Since each point-of-load converter supplies only a fraction of the computer's total power, its power handling capabilities can be much less than a centralized power supply. Smaller power handling requirements allow fabrication techniques which yield a higher component

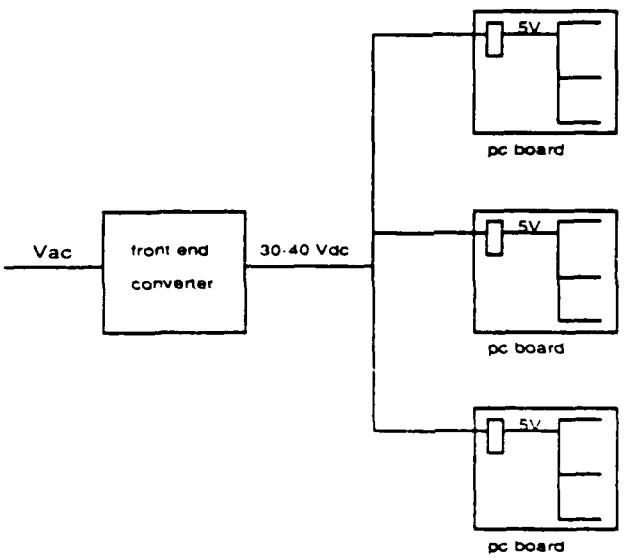


Figure 1.1: Point-of-Load Power Supply Architecture

packing density. Furthermore, once voltage regulation is accomplished at the logic board by a point-of-load converter, the voltage on the distribution bus can be raised. With a higher voltage, the bus can deliver the same power at a lower current, which permits smaller distribution busswork.

In order for a point-of-load conversion architecture to be viable, the individual power modules must be very small to minimize the required space on the computer logic boards. The largest components of the power modules are the capacitors and inductors which provide passive filtering. In order to reduce the size of the filtering elements while still maintaining the required filtering, the switching frequency of the module must be raised. The gains

achieved by raising the switching frequency and reducing the size of the filtering elements are lost if the required control circuitry must be implemented with numerous discrete components. Therefore, the modules' control circuitry must be integrated on a single chip. The first prototype point-of-load converters developed at MIT incorporated commercially available control chips. However, more recent research is considering even higher switching frequencies to further decrease the size of passive filter components. Consequently, the current research outstrips the performance capabilities of commercially available control IC's. Not wanting to lose the size and performance advantages of integrated control devices, the need arises for the design and fabrication of custom integrated control IC's.

1.1 Feedback Controller

Figure 1.2 depicts the general topology of the point-of-load DC-to-DC switching power supplies designed at MIT. The modules convert an input power at 30-50 Volts DC to an output power at 5 Volts DC. Primary side switches produce a square-wave waveform that is applied to the primary winding of a transformer. Diodes on the secondary side then rectify this waveform to get a DC waveform for the output. The output filter removes the unwanted AC components of the switching frequency and delivers only the DC component to the load. A feedback loop is closed around the system to keep the output voltage constant at 5 Volts regardless of changes in load conditions.

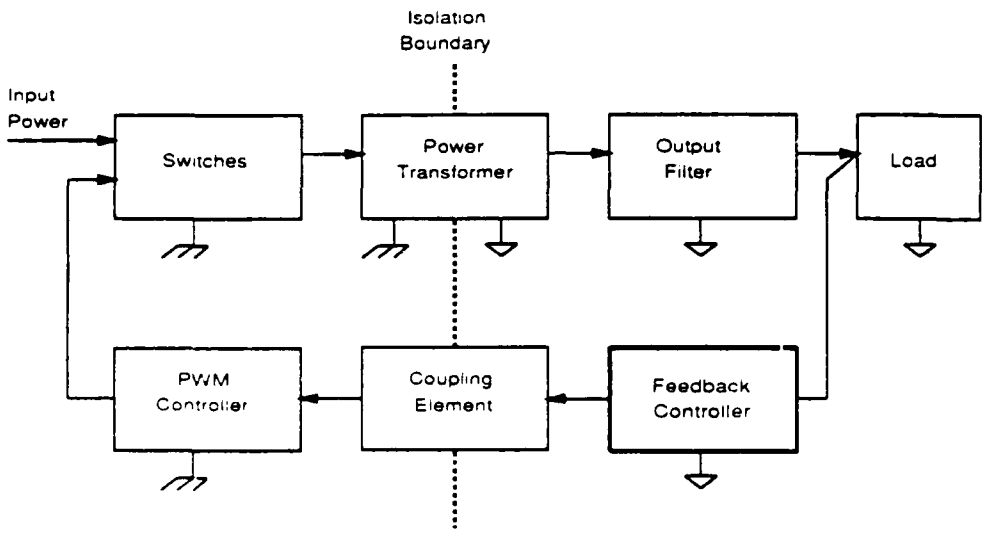


Figure 1.2: Switching Power Supply Topology

Industry standards require that the primary and secondary sides of the converter be electrically isolated from each other. The power transformer isolates the forward path, but some other coupling element must isolate the feedback path. Coupling elements currently under consideration at MIT include transformers, capacitors, and optoisolators. The feedback controller circuitry in the loop must measure the output voltage of the converter and provide an error signal that is suitable for each of the isolation devices. In general, the controller measures the DC output of the converter and applies a proportional AC signal to the isolation boundary.

Since miniaturized point-of-load converters necessitate small,

high-performance components, the feedback controller circuitry must be integrated on a single chip. The commercially available feedback controller IC's utilize a bipolar technology. Another available technology used extensively in VLSI applications is Complementary Metal Oxide Silicon, or CMOS. In order to encourage the development of prototype IC's, the Defense Advanced Research Projects Agency (DARPA) created the Metal Oxide Semiconductor Implementation Service, commonly referred to as MOSIS. MOSIS collects designs from multiple users and then fabricates a small number of parts for each user. Thus, by sharing the mask and wafer fabrication costs, MOSIS can quickly produce a small number of prototype IC's for each user at about one-tenth the normal cost. MOSIS supports primarily the CMOS technology.

Thus, given the need for custom control IC's and the availability and convenience of the MOSIS program, this thesis investigates the implementation of a feedback controller in the CMOS technology. The feedback controller provides a means to understand the capabilities and limitations of CMOS technology for power supply control circuitry, and also affords a comparison between CMOS control IC's and the commercially available circuits implemented in bipolar technology.

1.2 Outline

This document reports on the design, simulation, and testing of a CMOS secondary-side feedback control IC. The next chapter presents the design

goals and circuit topologies chosen to meet those goals. Chapter 3 reviews the results of HSPICE simulations of the IC's functional sub-cells. Chapter 4 addresses layout and fabrication concerns and presents results of some innovative IC repair using a focused ion beam. Chapter 5 details the performance of the circuits fabricated by MOSIS. Chapter 6 draws conclusions about the suitability of CMOS integrated circuits for power supply control and provides recommendations for future work.

Chapter 2

Design

2.1 Background

The function of the control circuitry in a switching DC-to-DC power supply is to maintain a constant output voltage. In order to regulate the output voltage with changes in load requirements, the converter output must be compared to an accurate reference voltage. The resulting error voltage must be amplified and fed back to the converter's control circuitry which will then correct the sensed error. In this way, as the load demand changes, the converter adapts to meet the new demand. The role of the feedback control IC can best be understood by considering the typical example as shown in Fig 2.1 [2].

The primary and secondary sides of the converter are electrically isolated from each other by means of a power transformer in the forward path and a small coupling transformer in the feedback path. The converter's 5 Volt output is divided down and compared to an on-chip precision 1.5 Volt refer-

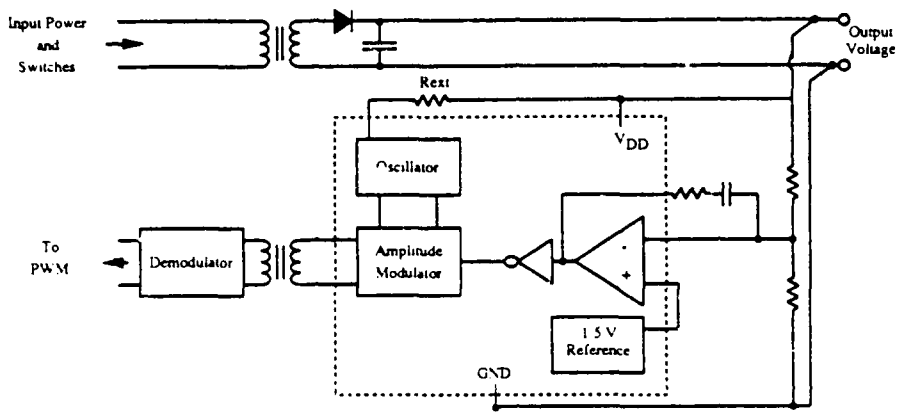


Figure 2.1: Typical Feedback Controller Application

ence. Before the error signal is applied to the amplitude modulator, it must be inverted for startup reasons. Since the Feedback Control IC is powered from the output voltage, when there is no output voltage (i.e. startup) the IC cannot send a signal. Thus, zero signal from the secondary side must correspond to the application of full power at the primary side. Hence, the need for an inverter before the amplitude modulator. The amplitude modulator receives a carrier signal from the on-chip oscillator and modulates the amplitude of that carrier wave based on the magnitude of the error signal. The amplitude-modulated AC signal is then transmitted across the isolation boundary via the coupling transformer. On the primary side, the error signal is demodulated and utilized to make corrections to the switching duty cycles of the converter.

Thus, the feedback controller IC consists of four main functional blocks: a precision voltage reference, an error amplifier, an oscillator, and an amplitude modulator. The design of the feedback controller investigates the suitability of CMOS for power supply control applications while striving to achieve design goals for each major functional block. The entire IC will be located on the secondary side of the converter and must thus function with a single 5 volt power supply and operate down to 4.5 Volts for proper converter startup. The precision reference must be both temperature and supply independent. The error amplifier must exhibit high common mode and power supply rejection and have reasonably large gain and bandwidth. Since a high frequency carrier signal reduces the required size of the coupling devices (transformers and capacitors), the oscillator must generate up to a 20 MHz carrier square wave with a 50% duty cycle. The frequency of oscillation must be externally controllable. Finally, the modulator must be capable of 20 MHz operation and have a high output current driving capability. These design goals strive to achieve in CMOS technology the performance of commercially available bipolar IC's while increasing the frequency of oscillation and output driving capabilities.

2.2 Voltage Reference

The first major component of the feedback controller is the voltage reference. The voltage reference determines the output voltage of the entire point-of-

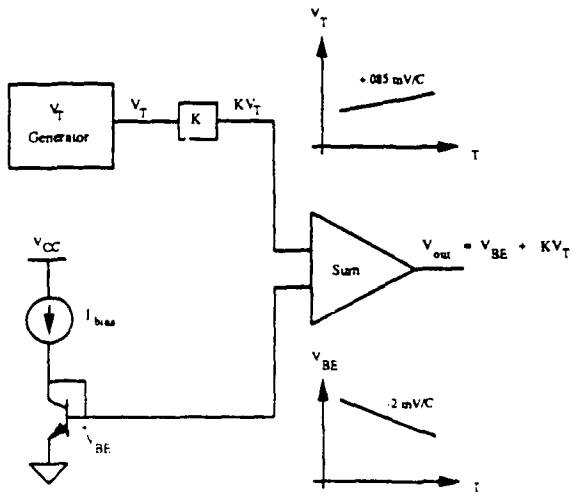


Figure 2.2: Bandgap Reference Circuit Topology

load power converter. Hence, the voltage reference circuitry must provide a very stable voltage over temperature. A circuit that is to first order temperature independent is a bandgap reference, shown in Fig. 2.2. The bandgap reference cancels the negative temperature coefficient of a p-n junction with the weighted positive temperature coefficient of the thermal voltage, V_T [3]. Although the CMOS process does not include bipolar devices, parasitic p-n junctions make implementation of bandgap references possible [6]. The output voltage is the sum of the two voltages,

$$V_{out} = V_{BE} + KV_T \tag{2.1}$$

Neglecting base current, the base-emitter voltage, V_{BE}, can be expressed

in terms of the bandgap voltage of silicon extrapolated to zero degrees Kelvin [5].

$$V_{BE} = V_{GO} - V_T[(\gamma - \alpha)\ln T - \ln EG] \tag{2.2}$$

where V_{GO} is the bandgap voltage, V_T is the thermal voltage $\left(\frac{kT}{q}\right)$, α is the temperature dependence of the bias current, γ is the temperature dependence of the electron mobility, and E and G are temperature independent constants. Substituting Eq. 2.2 into Eq. 2.1,

$$V_{out} = V_{GO} - V_T(\gamma - \alpha)\ln T + V_T(K + \ln EG) \tag{2.3}$$

The goal of the bandgap reference is temperature independence. Thus, the derivative of V_{out} with respect to temperature is set to zero.

$$\left.\frac{dV_{out}}{dT}\right|_{T=T_0} = \frac{V_{T0}}{T_0}(K + \ln EG) - \frac{V_{T0}}{T_0}(\gamma - \alpha)\ln T_0 - \frac{V_{T0}}{T_0}(\gamma - \alpha) = 0$$

which gives

$$(K + \ln EG) = (\gamma - \alpha)\ln T_0 + (\gamma - \alpha) \tag{2.4}$$

Substituting Eq. 2.4 back into the expression for V_{out} in Eq. 2.3 results in

$$V_{out}(T) = V_{GO} + V_T(\gamma - \alpha)\left(1 + \ln\frac{T_0}{T}\right) \tag{2.5}$$

Typically, $(\gamma - \alpha) = 2.2$ [5].

As Eq. 2.5 shows, V_{out} is still a function of temperature. However, the temperature coefficient is small and there exists one temperature where the temperature coefficient is zero, namely T_0. At $T = T_0$, $\frac{dV_{out}}{dT} = 0$. The

smallest temperature dependence occurs when T_0 corresponds to the operating temperature of the circuit. Designing to achieve first order temperature independence at 25°C, the "magic voltage" value of V_{out} is:

$$V_{out}(T)|_{T=25°C} = V_{GO} + 2.2V_{T0} = 1.2622\,V$$

2.2.1 Circuit Implementation

The standard CMOS bandgap reference circuit in Fig. 2.3 cancels the negative V_{BE} temperature coefficient with the positive temperature coefficient of the thermal voltage to achieve the "magic voltage" of 1.2622 volts [5]. The circuit was designed with a magic voltage of 1.2622 in order to be temperature independent at 25°C .

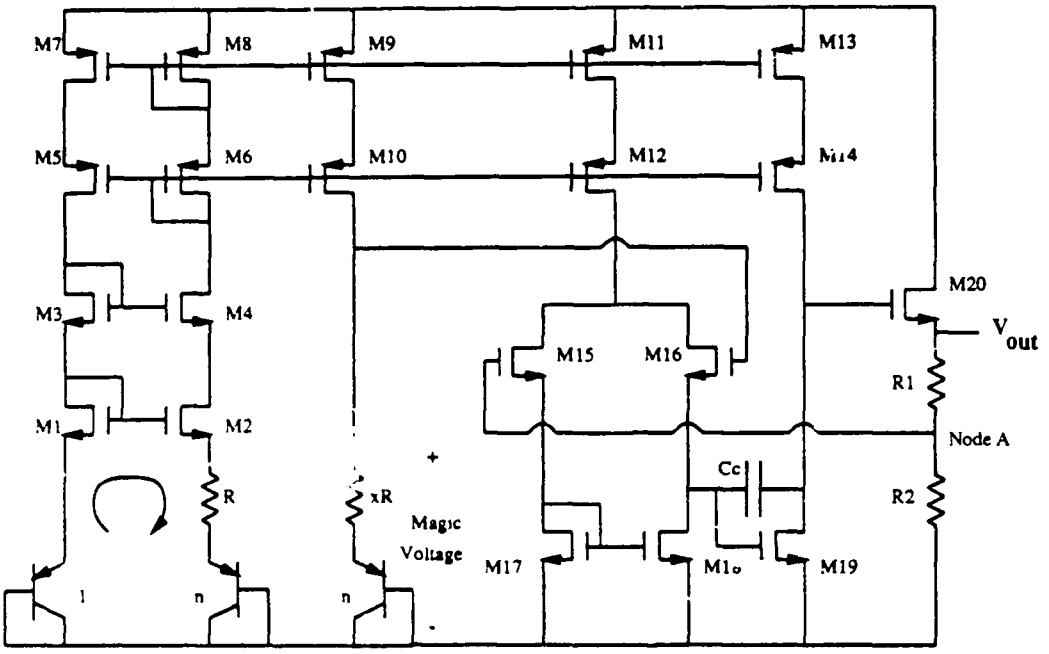
The left-hand side of the circuit generates a V_T-referenced current. Writing KVL equations around the loop as shown in Fig. 2.3

$$V_{BE_1} + V_{GS_1} = V_{GS_2} + V_R + V_{BE_n} \tag{2.6}$$

The rest of the circuitry above this loop is a current mirror that ensures that the current in the two legs are equal. Since the currents are equal, $V_{GS_1} = V_{GS_2}$ and

$$V_R = V_{BE_1} - V_{BE_n} \tag{2.7}$$

In terms of the bias current, I , Eq. 2.7 becomes



Devices	W/L
M1-M4	400/3
M5-M10	900/3
M11-M14	450/3
M15-M16	100/2
M17-M18	32/2
M19	64/2
M30	270/2

Figure 2.3: Bandgap Voltage Reference Schematic

$$IR = \frac{kT}{q} \ln \frac{I}{I_{s_1}} - \frac{kT}{q} \ln \frac{I}{I_{s_n}} \tag{2.8}$$

$$IR = \frac{kT}{q} \ln \frac{I_{s_1}}{I_{s_n}} \tag{2.9}$$

$$I = \frac{V_T \ln n}{R} \tag{2.10}$$

This current is mirrored to the third leg to generate the actual voltage reference.

$$V_{out} = V_{BE} + (x \ln n) V_T \tag{2.11}$$

In order to make this output voltage temperature independent at 25°C , the values of n and x were calculated to set V_{out} equal to 1.2622 Volts, the "magic voltage" calculated in the previous section. A bias current of $45\mu A$ results in a $V_{BE} = 0.5$ V. Choosing $n = 49$ for layout convenience results in $x = 7.85$ in order to achieve the design voltage of 1.2622 volts.

Given the temperature independent voltage of 1.2622 Volts, the op amp follower circuit generates a temperature independent voltage of 1.5 Volts. The resistor ratio, $R_2 = 5.3R_1$, insures that the 1.2622 Volts at node A produces a final output voltage of 1.5 Volts.

2.2.2 Design Considerations

In addition to choosing the size ratios necessary to implement the "magic voltage", design of the bandgap reference involves two other major considerations, namely biasing and matching [7]. Because the feedback control IC is located on the secondary side of the transformer and is hence powered by the very 5 V signal it is regulating, startup conditions present added difficulties in biasing. In order to provide adequate control at startup, the reference voltage needs to operate with a power supply down to 4.5 V. The large-signal device behavior of a MOSFET can be approximately modeled by [8]

$$I_D = \begin{cases} \frac{K'}{2}\left(\frac{W}{L}\right)\left[2(V_{gs}-V_t)V_{ds}-V_{ds}^2\right] & V_{ds} < (V_{gs}-V_t) \quad (a) \\ \frac{K'}{2}\left(\frac{W}{L}\right)(V_{gs}-V_t)^2 & V_{ds} > (V_{gs}-V_t) \quad (b) \end{cases} \tag{2.12}$$

where V_t is the threshold voltage, and K' is a measure of the conductivity of the inversion layer of the device that can be expressed as

$$K' = \frac{\mu\epsilon_{ox}}{t_{ox}} \tag{2.13}$$

In order for transistors M1-M8 to behave properly as current mirrors, they must be biased in the saturation or pinch-off region, with V_{DS} greater than $(V_{GS}-V_t)$. For a given current, a larger W/L ratio facilitates a smaller value of $(V_{GS}-V_t)$. Hence, a large W/L ratio is required for devices M1-M8 to be biased in saturation with a power supply rail down to 4.5 volts.

The second important design consideration is matching. The bandgap circuit theory hinges on the assumption that the currents in the three circuit legs are equal. Transistor nonidealities affect this assumption. Ideally,

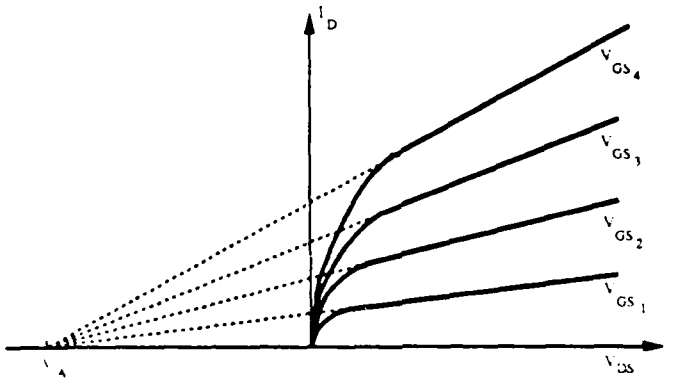


Figure 2.4 Actual Current-Voltage Characteristics of an n-channel MOSFET

MOSFETs in saturation will have the same drain current for a given V_{GS}, regardless of V_{DS}. However, actual I_D vs. V_{DS} curves exhibit a slope that is characterized by the Early voltage, V_A, as shown in Fig. 2.4 [9]. Since not all of the transistors in the current mirrors have the same V_{DS}, the solution is to set the bias at a very low I_D where the slope is minimal. Conveniently, low bias current also helps the 4.5 V biasing problem.

Process variations also affect current matching. Theoretically, identical transistors should mirror identical currents. However, manufacturing process variations produce non-identical transistors. The lengths of the current mirror devices were increased to 3 microns rather than the minimum possible length of 2 microns In this way, the W/L ratios are less susceptible to variations in the processing parameters.

2.3 Oscillator

As the high-density power conversion program at MIT strove to achieve greater packing density at higher frequencies, the need for custom controller IC's became apparent. Early researchers realized that as the program evolved, the required control IC's would have to be developed and optimized for each converter application. However, in order to avoid unnecessary duplication of IC design effort, the early MIT IC designers created a library of standard functional building blocks which could be readily included in subsequent designs [10]. The library, developed and pioneered primarily by Dr. Leo Casey, contained a variety of functional circuits implemented in the 3 micron CMOS process. However, due to the scalable nature of CMOS, the existing circuits could be readily implemented in a 2 micron process as well. The oscillator used in this work is a combination of standard and modified subcells drawn from Dr. Casey's control circuit library. The library assumed a 10 V power supply and so it required slight modification to operate with a 5 V supply.

The internal oscillator of the feedback control IC must supply a two-phase square wave with a 50% duty cycle. Dr. Casey successfully accomplished this task using three components from the control circuit library: a Schmitt trigger oscillator, a divider, and a phase splitter [10]. Fig. 2.5 shows his oscillator architecture schematically. The Schmitt trigger oscillator produces a simple square wave at twice the desired frequency. The divider divides the

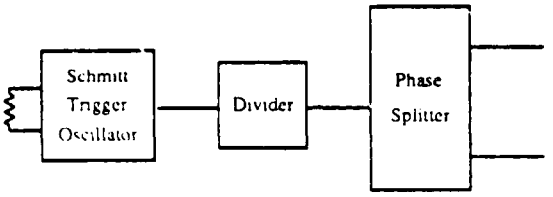


Figure 2.5: Oscillator Block Diagram

frequency of oscillation by two while insuring a 50% duty cycle. The phase splitter produces two square waves 180 degrees out of phase with each other.

2.3.1 Schmitt Trigger Oscillator

Figure 2.6 depicts the Schmitt trigger oscillator. Initially, the Schmitt trigger output is a low signal and the top current source is charging the capacitor. When the voltage on the capacitor reaches the upper threshold of the Schmitt trigger, the output switches from low to high, the top current source is switched out and the bottom current source is switched in. The bottom source discharges the capacitor until the voltage on the capacitor falls below the lower threshold of the Schmitt trigger and the cycle starts again. Since the value of C is fixed by the on-chip capacitor, the frequency of oscillation is controlled by the current sources.

Current Source Design

The goal of the current sources in the Schmitt trigger oscillator is to provide a means of externally varying the frequency of oscillation. Figure 2.7 shows

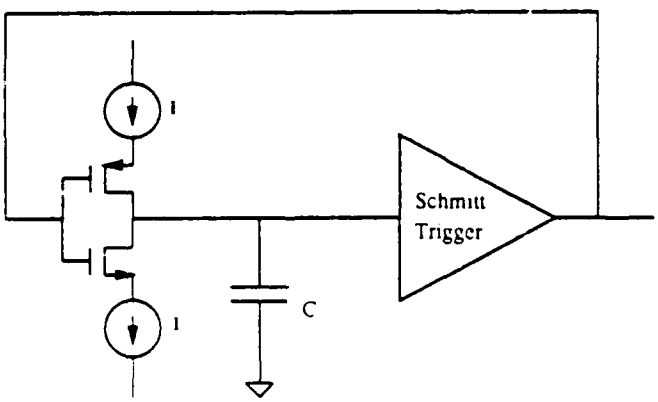


Figure 2.6: Schmitt Trigger Oscillator Block Diagram

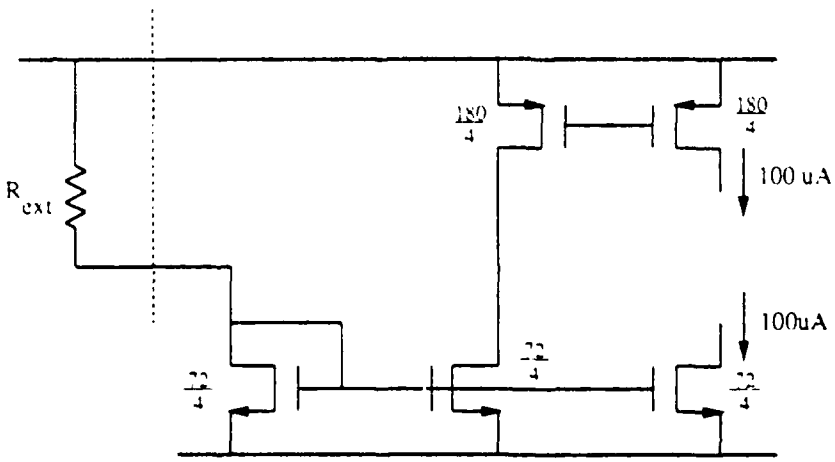


Figure 2.7: Current Source Circuit

the current source topology. The voltage drop across the external resistor provides a reference current that is then mirrored to the top and bottom current sources. The external resistor provides a means to vary the current in the current sources and directly vary the frequency of oscillation. Assuming a 3 V difference in switching levels of the Schmitt trigger and a 400 fF capacitor, a current of 100μA is required for 40 MHz operation. The voltage across the resistor and diode-connected MOSFET equals the supply voltage,

$$V_{DD} = I_D R + V_{GS} \tag{2.14}$$

Using Eq. 2.12 to eliminate V_{gs},

$$V_{DD} = I_D R + V_t + \sqrt{\frac{2I_D}{K'\left(\frac{W}{L}\right)}} \tag{2.15}$$

Choosing an external resistor of 33kΩ and setting I_D equal to 100μA results in $\frac{W}{L}$ =18 as shown in Fig. 2.7. The W/L of the p-channel devices reflect the K_n' K_p' ratio of approximately 2.5 which is typical of MOSIS fabrication.

Schmitt Trigger Design

As depicted in Fig. 2.6 the current source charges or discharges the capacitor as determined by the output of the Schmitt trigger. Figure 2.8 shows the basic Schmitt trigger topology. The Schmitt trigger consists of two inverters with pullup and pulldown transistors to separate the low-to-high and high-to-low transitions. Stepping through the operation of the circuit, when the

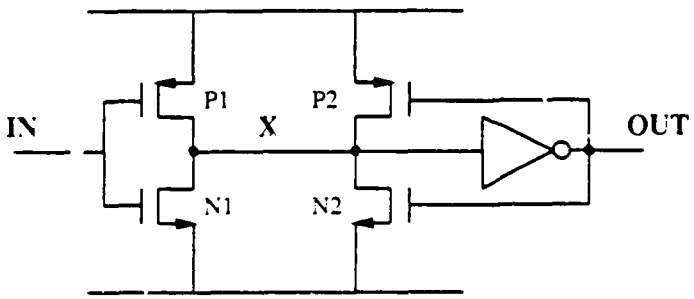


Figure 2.8: Schmitt Trigger Topology

input is low, the output of the second inverter is also low, turning on the pullup device P2. Conversely, when the input is high, the output is also high, turning on the pulldown device N2. It is the pullup and pulldown devices that separate the switching thresholds of the Schmitt trigger. Starting with the output low and P2 on, when the input goes from low to high, Node X cannot decrease in voltage until N1 picks up all of the current in both P1 and the pullup device, P2. Or, until

$$I_{N1} = I_{P1} + I_{P2} \tag{2.16}$$

Likewise with the output high and N2 on, when the input goes low, Node X cannot increase in voltage until the current in P1 equals that in both N1 and and the pulldown device, N2.

$$I_{P1} = I_{N1} + I_{N2} \tag{2.17}$$

Substituting the large signal current relationships of Eq. 2.12 into Eqs. 2.16 and 2.17 results in

$$\left(\frac{W}{L}\right)_{N1} K'_n(V_G - V_{tn})^2 = \left(\frac{W}{L}\right)_{P1} K'_p(V_{DD} - V_G + V_{tp})^2 + \left(\frac{W}{L}\right)_{P2} K'_p(V_{DD} + V_{tp})^2 \tag{2.18}$$

$$\left(\frac{W}{L}\right)_{P1} K'_p(V_{DD} - V_G + V_{tp})^2 = \left(\frac{W}{L}\right)_{N1} K'_n(V_{DD} + V_{tn})^2 + \left(\frac{W}{L}\right)_{N2} K'_n(V_{DD} + V_{tn})^2 \tag{2.19}$$

Choosing switching levels of 4 V and 1 V and assuming $V_{tn} \simeq -V_{tp} \simeq 1V$, and $K'_n / K'_p = 2.5$, Eqs. 2.18 and 2.19 reduce to

$$\left(\frac{W}{L}\right)_{N1} \simeq 1.4 \left(\frac{W}{L}\right)_{P2} \tag{2.20}$$

$$\left(\frac{W}{L}\right)_{P1} \simeq 4.4 \left(\frac{W}{L}\right)_{N2} \tag{2.21}$$

These rough sizing calculations were confirmed by a more accurate HSPICE simulation. The ratios were similar to those developed by Dr. Casey, but, the different power supply requirements and subsequent changes in switching thresholds scaled the ratios slightly [10]. Figure 2.9 shows the complete Schmitt trigger oscillator.

2.3.2 Divider

The goal of the divider circuit is to obtain a completely symmetric output signal. The divider circuit implemented in the feedback control IC is based on a very similar divider circuit in Dr. Casey's circuit library. By a combination of digital logic circuits, the library circuit nearly attained a symmetric

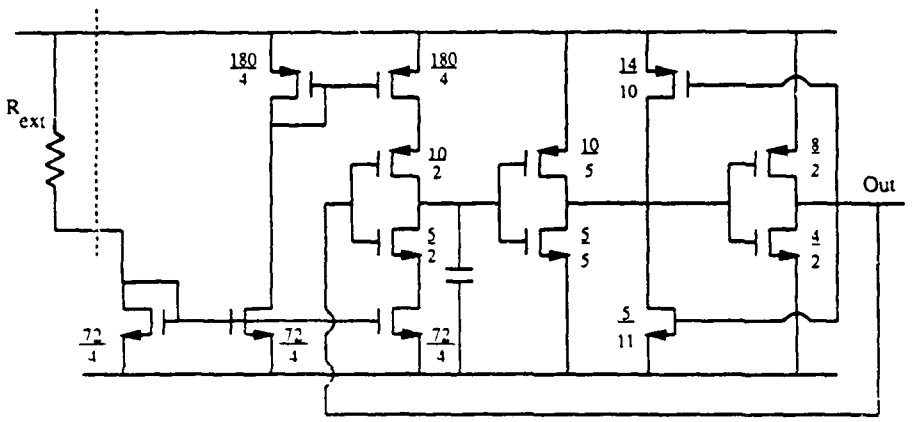


Figure 2.9: Circuit Implementation of Schmitt Trigger Oscillator

output waveform [10]. However, a difference of one gate delay provided a small degree of asymmetry. Dr. Casey recognized the delay and proposed an alternate design to achieve symmetry. The divider circuit included here incorporates the improved design.

The divider circuit is a Master-Slave J-K Flip-Flop as shown in the logic schematic of Fig. 2.10. The heart of the circuit is the Set-Reset or S-R latch. When the S input is active, the output, Q, goes low. When the R input is active, Q goes high. The output of the second S-R latch in Fig. 2.10 is the divider output. The rest of the Master-Slave topology ensures that the inputs to the second latch (labeled S' and R' in Fig. 2.10) alternate with every rising edge of the input clock. Ideally, the output is a 50% Duty cycle square wave at one-half the frequency of the input clock. However, the digital logic

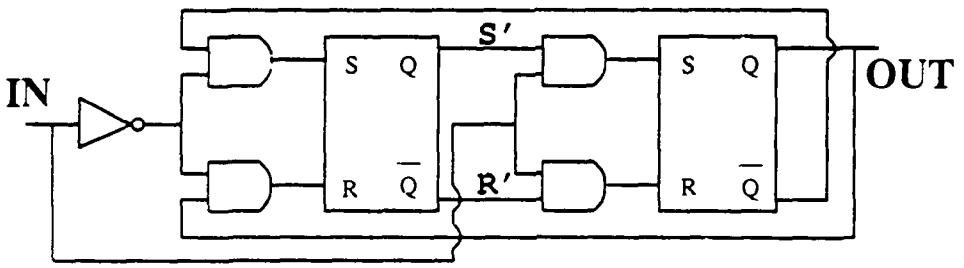
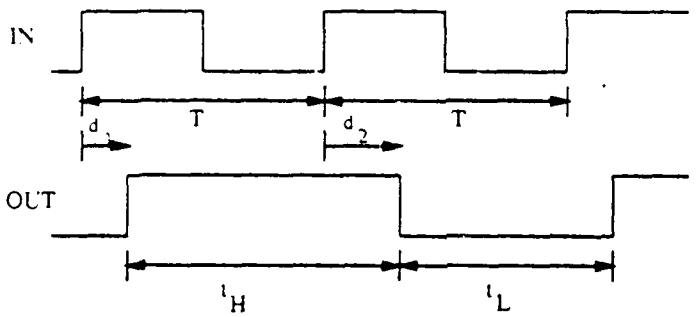


Figure 2.10: Master-Slave J-K Flip-Flop



$$t_H = T - d_1 + d_2$$

$$t_L = T - d_2 + d_1$$

$$t_H - t_L = 2(d_1 - d_2)$$

Figure 2.11: Asymmetrical Divider Output

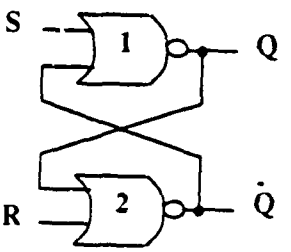
circuits introduce a delay between input an output. Asymmetry is the result of the delays as shown in Fig. 2.11. The difference in duration of a high and low output signal is twice the difference in delays. Examining the Master-Slave J-K Flip-Flop reveals that the delays of the final latch determine the delays of the divider. If the delay from an S input to a low output is not the same as the delay from an R input to a high output, the output signal will be asymmetric.

The S-R latch originally used in Dr. Casey's divider circuit utilized a pair of cross-coupled NOR gates as shown in Fig. 2.12 [10]. Assuming an identical delay of d for each NOR gate, the delay from an S input to a Q output is d, the delay through gate 1. However, the delay from a R input to a Q output is $2d$, the delay through gate 2 and and the delay through gate 2. The result is an asymmetrical output.

The improved design incorporates cross-coupled NAND gates appropriately scaled to match delay times, as shown in Fig. 2.13. Assuming a $K'_n/K'_p \simeq 2$, the on-state resistance, R, of a p-channel MOSFET will be approximately twice that of an n-channel. Thus, the delay from an R input (active low) to a Q output is

$$(2R)C_{load} + (R + R)C_{load} = 4RC_{load} \tag{2.22}$$

Without additional scaling, the pullup delay of an S input to a Q output would be $2RC_{load}$. However, halving the width of the pullup transistor (as



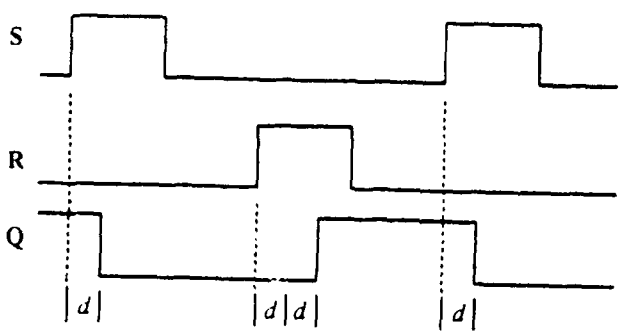


Figure 2.12: NOR Gate S-R Latch

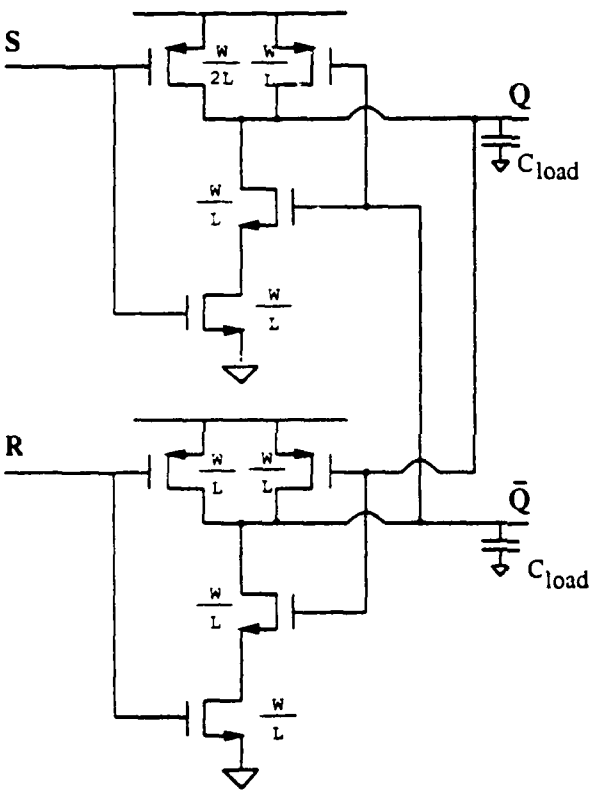


Figure 2.13: Scaled NAND Gate S-R Latch

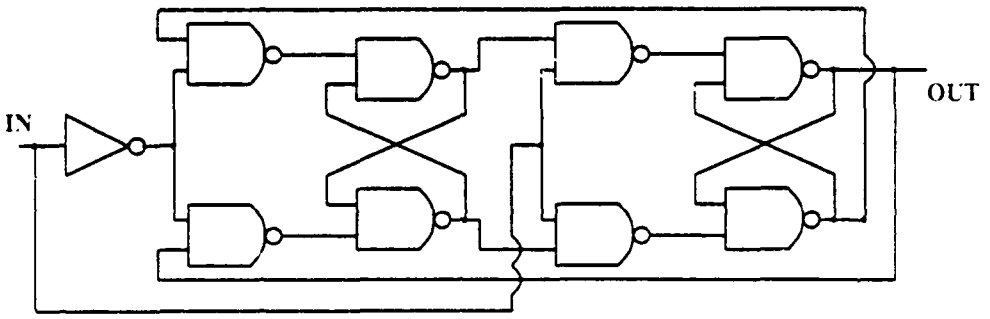


Figure 2.14: Improved Master-Slave J-K Flip-Flop

seen in Fig. 2.13) doubles the resistance resulting in a time delay of $4RC_{load}$, balancing the delays. The improved S-R latch slightly modifies the logic diagram of the Master-Slave J-K Flip-Flop, as shown in Fig. 2.14.

2.3.3 Phase Splitter

The goal of the phase splitter is to extract two perfectly out-of-phase square waves from a single input square wave. The block diagram of the phase splitter is shown in Fig 2.15. Because one path has one more inverter than the other, the two outputs are out of phase. If the delays of the two signal paths are equal, the signals will be exactly 180 degrees out of phase. The objective of the design was to balance the two delay paths.

The proper scaling ratios were determined by considering each unit-width of an inverter stage to have a resistance, r, and capacitance, c. The inverters in the two-inverter path were scaled equally making the first inverter b units

wide and the second inverter b^2 units wide. Likewise, the first two inverters in the three-inverter path were scaled equally, a and a^2, as shown in Fig. 2.15. In order to make the output impedance of both paths equal, the third inverter was given a unit width of b^2, as well. Given these scaling factors, Fig. 2.15 shows the input capacitance of each inverter as the product of its width and the unit capacitance, c. The output resistance is the unit resistance divided by the width.

An estimate of the total delay through each path is the sum of the RC products of each stage. Equating the delays in the two paths yields

$$\left(\frac{r}{a}\right) a^2 c + \left(\frac{r}{a^2}\right) b^2 c = \left(\frac{r}{b}\right) b^2 c \tag{2.23}$$

$$arc + \left(\frac{b}{a}\right)^2 rc = brc \tag{2.24}$$

Factoring out an rc product and simplifying

$$a^3 - a^2 b + b^2 = 0 \tag{2.25}$$

Many pairs of numbers, $(a : b)$, satisfy Eq. 2.25. Layout design rules dictate whole number solutions such as (4:8), (5:7), (5:18), and so on. Since the absolute value of the time delay is proportional to the value of b, the pair with the smallest value of b, (5:7), was chosen. The resulting phase splitter circuit is shown in Fig. 2.16

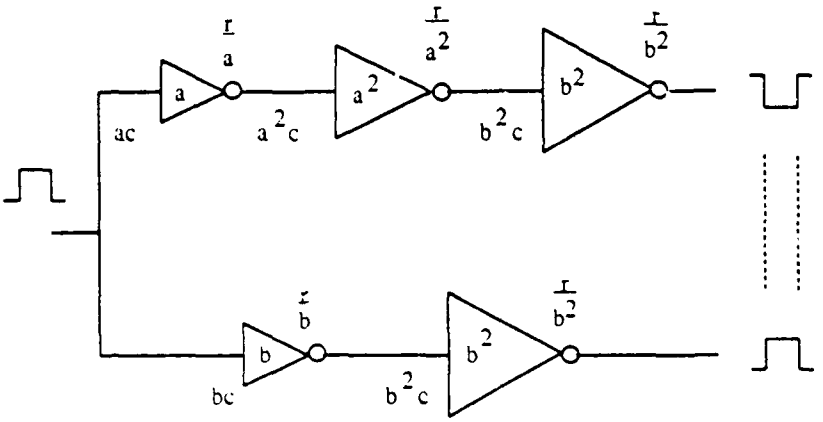


Figure 2.15: Block Diagram of Phase Splitter

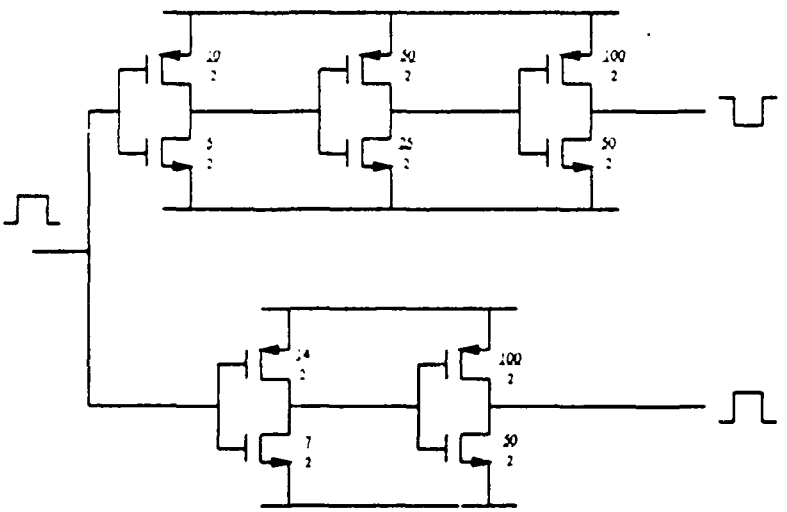


Figure 2.16. Phase Splitter Circuit

2.4 Error Amplifier

The error amplifier is s high performance operational amplifier with a moderate gain and large bandwidth. The gain must be high enough to accommodate DC offsets in the feedback path. A large bandwidth gives the power supply designer flexibility in closing the feedback loop. Additionally, a primary concern in the amplifier design is the power supply rejection. The positive power supply of the amplifier is the 5 V output of the power converter-the very signal it is measuring. Thus, the amplifier must have high power supply rejection. Similarly, the common mode rejection of the amplifier is also an important design consideration. The amplifier output must reflect a difference in the input signals while rejecting common inputs.

The standard CMOS op amp as shown in Fig. 2.17 does not adequately reject power supply noise [4]. The compensation capacitor, C_c, is required to ensure closed-loop stability. However, the compensation capacitor results in poor rejection of power supply noise [11]. At high frequencies, the compensation capacitor nearly shorts the drain and gate of M5 together. The incremental output voltage to a power supply noise signal, v_n, is

$$\Delta v_{out} = v_n + \Delta v_{GS_8} \tag{2.26}$$

A constant bias current, I, dictates a constant V_{GS}, thus $\Delta v_{GS_8} = 0$ so that

$$\Delta v_{out} = v_n \tag{2.27}$$

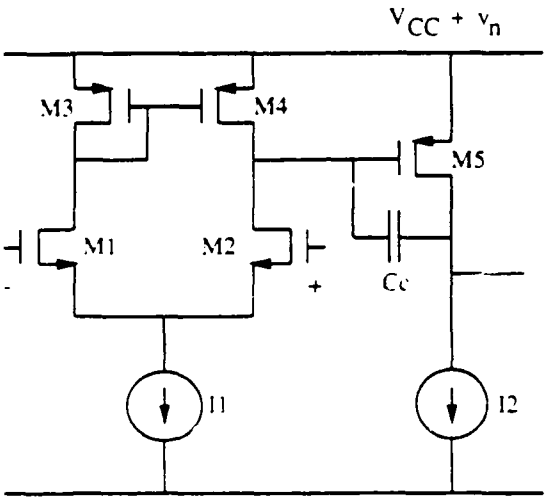


Figure 2.17. Standard CMOS Operational Amplifier Topology

and the power supply noise is coupled directly to the output signal.

An alternate op amp topology shown in Fig. 2.18 avoids the compensation capacitor degradation of the power supply rejection [11]. The modified circuit requires compensation by means of the load capacitor, C_L, which does not affect the power supply rejection at high frequencies. This folded cascode topology was selected for the error amplifier.

2.4.1 Small signal analysis

The folded cascode topology achieves a high bandwidth by utilizing the familiar cascode configuration to overcome the Miller capacitance. The cascode advantage can best be demonstrated by considering the simple common

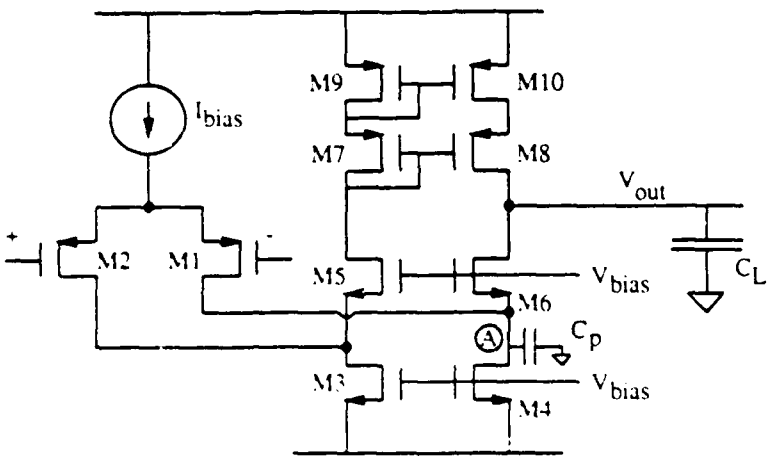


Figure 2.18 Folded Cascode Operational Amplifier

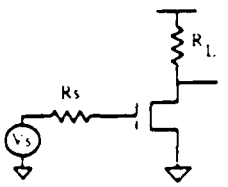


Figure 2.19 Simplified Common Source Amplifier Circuit

source amplifier shown in Fig. 2.19. Assuming the device is biased in saturation, the simplified small signal model of the circuit shown in Fig. 2.20 results. The dominant time constant associated with the gate to drain capacitance, C_{gd}, (also known as the Miller capacitance) is [5]

$$\tau_{C_{gd}} = C_{gd}(R_S + R_L + g_m R_S R_L) \tag{2.28}$$

However, the cascode topology shown in Fig. 2.21 decreases this time con-

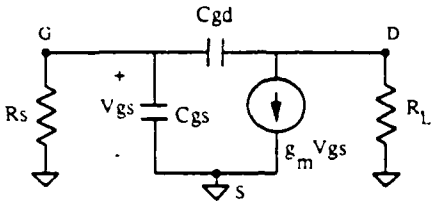


Figure 2.20: Incremental Model of Common Source Amplifier

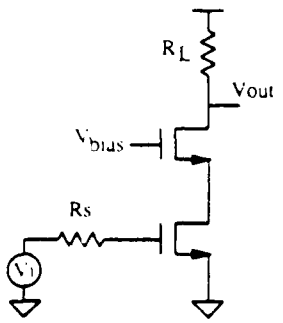


Figure 2.21. Cascoded Common Source Amplifier Circuit

stant significantly. The resulting small signal model is shown in Fig. 2.22. The two resulting time constants due to C_{gd} are

$$\tau_{C_{gd1}} = C_{gd1}(R_S + \frac{1}{g_{m1}} + g_m \frac{1}{g_m} R_S) \simeq C_{gd1}(2R_S) \tag{2.29}$$

$$\tau_{C_{gd2}} = C_{gd2}(R_L) \tag{2.30}$$

$$\tau_{C_{gd1}} + \tau_{C_{gd2}} \simeq C_{gd}(2R_S + R_L) \tag{2.31}$$

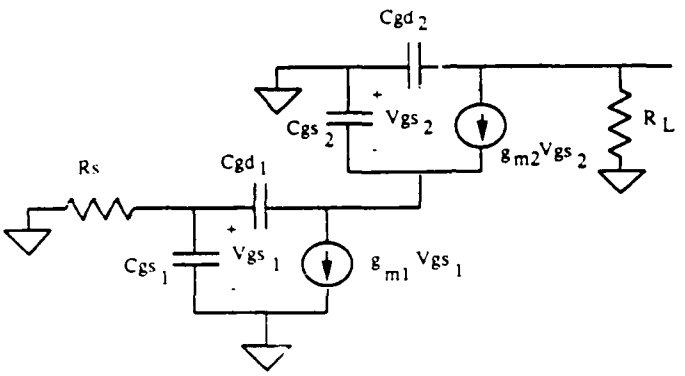


Figure 2.22. Incremental Model of Cascoded Common Source Amplifier

The cascode configuration avoids the $R_L R_S$ product, greatly reducing the associated time constants and hence, increasing the bandwidth.

The folded cascode operational amplifier shown in Fig. 2.18 combines a p-channel device, M1, with the n-channel device, M6, in a common base stage to form a "folded-over" cascode stage. Similar to the common source amplifier of Fig. 2.21, the gain of the folded cascode amplifier is $g_m R_L$. The load resistance, R_L, is the output impedance, R_o. Figure 2.23 shows the incremental model of M1 and M6 used to determine the output impedance. Injecting a test current, i_x,

$$i_x = i_1 + g_{m_6} v_{gs_6} \tag{2.32}$$

$$i_x = i_1 + g_{m_6}(-i_x r_{o_1}) \tag{2.33}$$

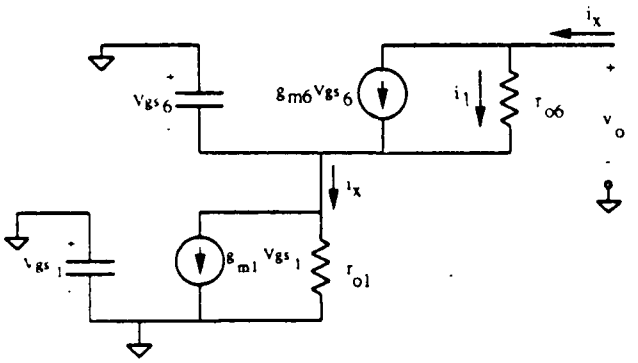


Figure 2.23: Small signal model used to determine output resistance

Solving for i_1

$$i_1 = (1 + g_{m_6} r_{o_1}) i_x \tag{2.34}$$

The output resistance is the output voltage divided by the test current. Solving for v_o

$$v_o = i_x r_{o_1} + i_1 r_{o_6} \tag{2.35}$$

$$v_o = i_x r_{o_1} + i_x (1 + g_{m_6} r_{o_1}) r_{o_6} \tag{2.36}$$

$$R_o = \frac{v_o}{i_x} = r_{o_1} + (1 + g_{m_6} r_{o_1}) r_{o_6} \simeq g_{m_6} r_{o_1} r_{o_6} \tag{2.37}$$

The gain of the amplifier is then

$$A_v = g_{m_1} R_o \simeq g_{m_1} g_{m_6} r_{o_1} r_{o_6} \tag{2.38}$$

2.4.2 Frequency response

The high output impedance, R_o, and the compensation capacitor, C_L, comprise the dominant time constant in the frequency response of the amplifier.

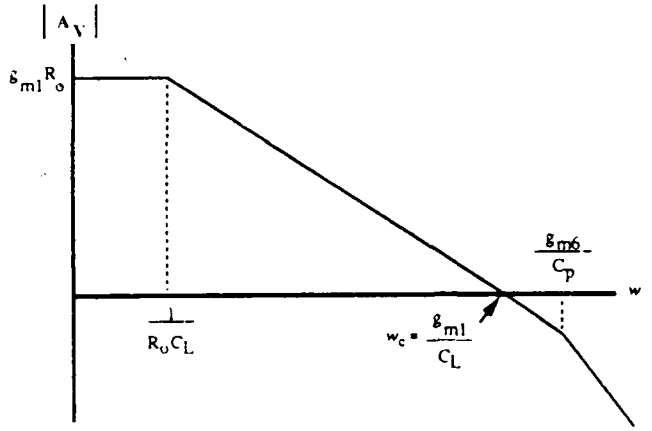


Figure 2.24: Frequency Response

The next nearest pole occurs at g_{m_6}/C_p, where C_p is the parasitic capacitance of node A as shown in Fig. 2.18. Increasing the output capacitance, C_L, increases the phase margin and hence the closed loop stability of the amplifier. Figure 2.24 shows a Bode plot of the amplifier's frequency response.

2.4.3 Design Considerations

The folded cascode op amp has the advantages of moderate gain, wide bandwidth, good phase margin, simple compensation, and a high power supply rejection ratio. The disadvantage of the topology is a decreased output signal swing due to the many cascaded devices at the output stage. The incremental models used to devise the gain and frequency response of the amplifier only apply for transistors in saturation, or as shown in Eq. 2.12, $V_{DS} > (V_{GS} - V_t)$.

Thus the output signal swing is limited by the V_{DS} needed to keep both sides of the output stage in saturation.

Cascode Biasing

The required V_{DS} bias voltage needed for the current mirror load of the amplifier is best understood by considering the cascoded current mirror shown in Fig. 2.25. Assuming the devices are in saturation, the drain current is governed by

$$I_D = \frac{K'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 \tag{2.39}$$

In order to be in saturation, $V_{DS} > (V_{GS} - V_t)$. Rearranging Eq. 2.39 gives

$$\Delta V = (V_{GS} - V_t) = \sqrt{\frac{I_D}{\frac{K'}{2}\left(\frac{W}{L}\right)}} \tag{2.40}$$

From Eq. 2.40, the gate to source voltage, V_{GS} is defined as

$$V_{GS} = V_t + \Delta V \tag{2.41}$$

Considering the cascoded current source of Fig. 2.25, the diode connected transistor, M1, is, by it's configuration, guaranteed to be in saturation, thus its V_{GS} is determined by Eq. 2.41. Assuming identical current in device, M2, the V_{DS} needed to keep it in saturation is

$$V_{DS} > V_{GS} - V_t \tag{2.42}$$

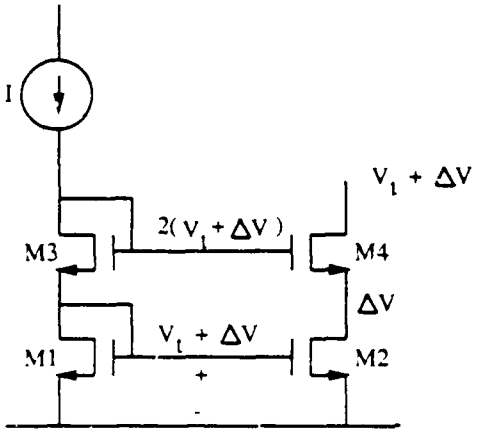


Figure 2.25: Cascoded Current Mirror

$$V_{DS} > (V_t + \Delta V) - V_t \tag{2.43}$$

$$V_{DS} > \Delta V \tag{2.44}$$

Similarly, identical current and identical size means that the the V_{GS} of device M3 is the same as M1, or $V_{GS} = (V_t + \Delta V)$. As shown in Fig 2.25, the gate voltage of the top mirror is then

$$V_{GS_1} - V_{GS_3} = 2(V_t + \Delta V) \tag{2.45}$$

Thus, in order for device, M4, to remain in saturation

$$V_{DS} > V_{GS} - V_t \tag{2.46}$$

$$V_{DS} > 2(V_t + \Delta V) - \Delta V - V_t \tag{2.47}$$

$$V_{DS} > V_t + \Delta V \tag{2.48}$$

Combining Eq. 2.44 and Eq. 2.48, in order for both M2 and M4 to remain in saturation, the output voltage, V_{out}, is limited by

$$V_{out} > V_t + \Delta V + \Delta V = V_t + 2\Delta V \tag{2.49}$$

With a reasonably large current a typical value for ΔV might be .4 V. With a threshold voltage of about a volt, V_{out} must be no less than 1.8 volts. If the cascoded stage is biased with a similar cascoded current mirror, the output swing of the amplifier would be limited to only 1.4 volts with 5 volt power supply rails. In order to achieve a larger output swing, an alternate biasing scheme must be utilized.

Improved Cascode Biasing

The improved cascode topology is shown in Fig. 2.26. The gate voltage of the bottom transistors is the same as the previous topology, $V_{GS} = (V_t + \Delta V)$. The difference in the two biasing networks is in the sizing of M3. As shown in Fig. 2.26, the size of M3 is W/4L. The current in M1 and M3 is the same, resulting in

$$\frac{1}{4}\frac{K'}{2}\frac{W}{L}(\Delta V_3)^2 = \frac{K'}{2}\frac{W}{L}(\Delta V_1)^2 \tag{2.50}$$

$$\frac{1}{4}(\Delta V_3)^2 = (\Delta V_1)^2 \tag{2.51}$$

$$\Delta V_3 = 2\Delta V_1 \tag{2.52}$$

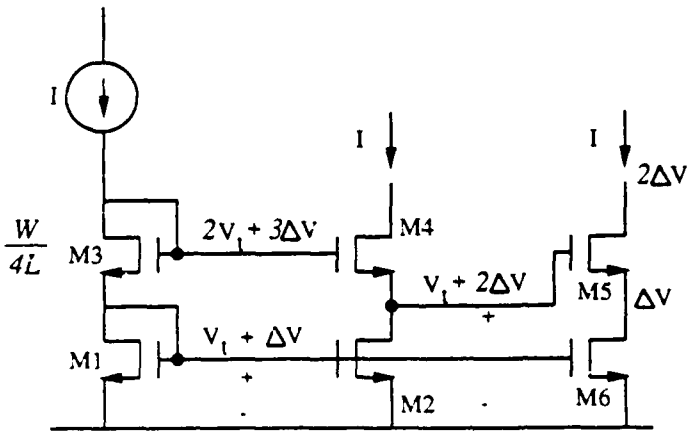


Figure 2.26: Improved Cascode Current Mirror

As shown in Fig. 2.26, the gate voltage of M3 is then $2V_t + 3\Delta V$, making the source voltage of M4 now

$$V_{GS} = \Delta V + V_t \tag{2.53}$$

$$2V_t + 3\Delta V - V_S = V_t + \Delta V \tag{2.54}$$

$$V_S = V_t + 2\Delta V \tag{2.55}$$

In order for device M6 to remain in saturation,

$$V_{DS} > V_{GS} - V_t \tag{2.56}$$

$$V_{DS} > (V_t + 2\Delta V) - \Delta V - V_t \tag{2.57}$$

$$V_{DS} > \Delta V \tag{2.58}$$

Thus, for the improved cascode biasing network, the output signal swing is limited by

$$V_{out} > 2\Delta V \tag{2.59}$$

The elimination on the threshold voltage by using this configuration provides an added volt of signal swing.

The improved cascode current source also benefits the common mode rejection of the amplifier. If the current source that biases the differential pair was a perfect current source, the current in M1 and M2 would be independent of the common mode voltage. Cascoding a simple one transistor current mirror increases the output impedance and decreases the mirror's sensitivity to changes in common mode voltages. Using a similar improved cascode current mirror biasing scheme for the differential current source provides a cascoded current source while still keeping the differential pair in saturation.

Sizing

As can be seen from the frequency response in Fig. 2.24, large values for both g_{m_1} and g_{m_6} contribute to a large gain and increased bandwidth. The transconductance of a MOSFET can be approximated by

$$g_m = \sqrt{2K'\left(\frac{W}{L}\right)I_D} \tag{2.60}$$

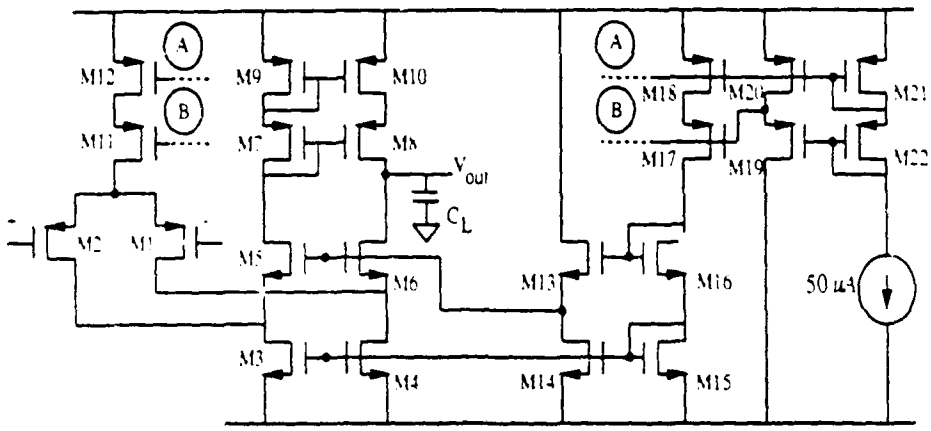
Equation 2.60 shows that increasing the bias current, I_D, would increase g_m. However, as Eq. 2.38 shows, the gain is also dependent upon the output impedance, R_o, which is governed by the output impedance of transistors M1 and M6. The output resistance of a MOSFET decreases with increasing bias current as evidenced by the increased slope of $I_D - V_{DS}$ curves of a nonideal MOSFET shown in Fig. 2.4. In terms of the Early voltage of the transistor, V_A, the output resistance is

$$r_o = \frac{V_A}{I_D} \tag{2.61}$$

Thus, increasing current does not necessarily increase gain. The g_m of both M1 and M6 can be increased, however, by increasing the W/L ratios. Simulation shows that the gain can be optimized with a large current in M1, a smaller current in M6, and large W/L ratios for both M1 and M6. The final amplifier circuit is shown in Fig. 2.27.

2.4.4 Startup Criteria

The startup conditions require that an additional component be added to the error amplifier. The error amplifier is generally configured as an integrator, as shown in Fig. 2.28. As the converter is starting up, and the secondary side feedback control IC is powering up, the 1.5 bandgap reference voltage stabilizes before the converter output reaches 5 volts. Thus, the positive input to the op amp will be greater than the negative input, driving the



Devices	W/L
M1-M2	480/2
M3-M10	240/2
M11-M12	270/2
M13-M15	80/2
M16	18/2
M17-M18	90/2
M19-M21	84/2
M22	18/2

Figure 2.27: Experimental Folded Cascode Operational Amplifier

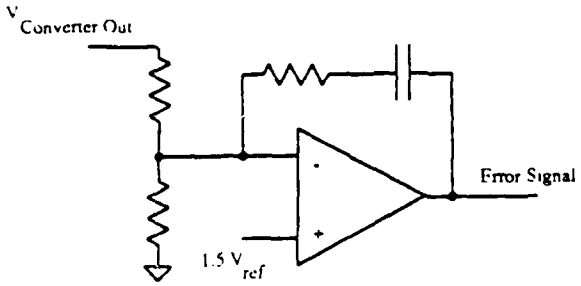


Figure 2.28 Typical Error Amplifier Configuration

output to the positive saturation of the op amp, since

$$V_o = A_v(v_+ - v_-) \tag{2.62}$$

where A_v is the open loop gain of the amplifier. The very large positive error signal is applied to the modulator and fed back across the isolation boundary to the primary side. The primary side switch controller interprets the high signal as an overshoot in the output and takes action to reduce the converter output voltage, effectively shutting the converter down. Proper startup requires that a low signal is returned when the input is below the desired voltage. Hence, the error amplifier signal must be inverted as shown in Fig. 2.29(a).

However, the folded cascode topology of the error amplifier produces a high-impedance output node. This is acceptable for driving the gates of successive stages since the input impedance of a Mosfet is essentially infinite. But in order to present a low impedance output node to the user for compensation purposes the output of the error amplifier must be buffered. Pushing

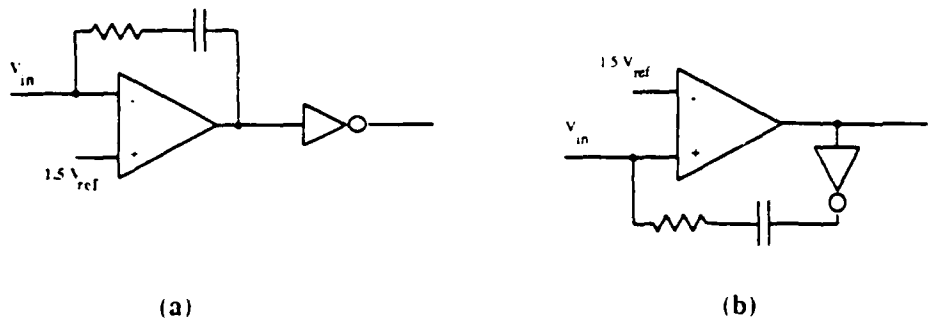
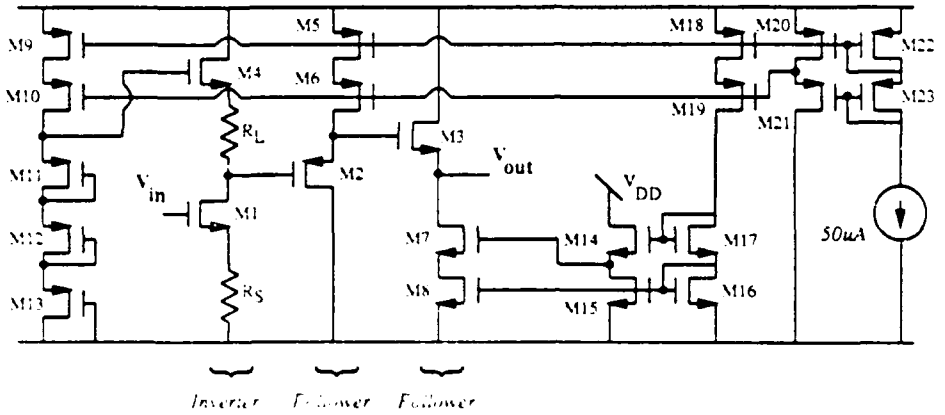


Figure 2.29 Integrators with Additional Inverter Required for Startup

the inverter into the feedback loop as shown in Fig. 2.29(b) provides both the necessary buffering and inverting functions.

The three stage implementation of the analog inverter is shown in Fig. 2.30. The gain of the first stage is R_L / R_S, slightly greater than one so that when combined with the followers, the overall gain is unity. The top transistor of the gain stage isolates the inverter from power supply fluctuations. The pair of followers buffer the output while nulling offset voltages. Although the inverting stage closely resembles the common source amplifier of Fig. 2.19, Miller capacitance does not significantly limit the bandwidth of the inverter stage due to its low g_m and near unity gain. The bandwidth limiting factor in the error amplifier-inverter combination is the error amplifier.



Devices	W/L
M1	20/2
M2	60/2
M3	128/2
M4	600/2
M5-M6	90/2
M7-M8	240/2
M9-M10	90/2
M11-M13	22/2
M14-M16	20/2
M17	5/2
M18-M19	90/2
M20-M22	84/2
M23	18/2
R_L	11 $K\Omega$
R_S	7 $K\Omega$

Figure 2.30 Inverter Circuit Schematic

2.5 Modulator

The error amplifier compares the input signal to the bandgap reference voltage to produce an error signal. Based on the error signal, the modulator must provide an AC signal which can then be applied to the isolation boundary. To implement the chosen amplitude modulation scheme, the modulator must impress the error signal on a carrier square wave generated by the oscillator. To take advantage of the oscillator design, the modulator must be able to operate with a 20 MHz carrier signal. The modulator could also augment the moderate gain of the amplifier by providing gain to the error signal. Finally, the modulator should have an output swing capability of at least 2.5 volts peak-to-peak and be able to sink and source at least 1.5 mA of current in order to be compatible with the isolation devices (transformers, capacitors, and optoisolators).

2.5.1 Circuit Implementation

Figure 2.31 depicts the double-balanced modulator circuit. The differential pair splits the bias current between the two legs of the modulator. The difference between the error amplifier operating point voltage and the bias voltage unbalances the current in the two legs of the modulator. The cross-coupled switches on top of the differential pair switch the currents back and forth between the load resistors to produce an AC signal. Changes in the error signal are reflected by changes in the amplitude of the signal. The

amplitude-modulated carrier signal is then buffered by an output stage and provided to external pins.

2.5.2 Design Considerations

The desired 2.5 volt output swing involves trading off bias current and load resistance. The maximum output swing occurs when one leg carries nearly all the bias current

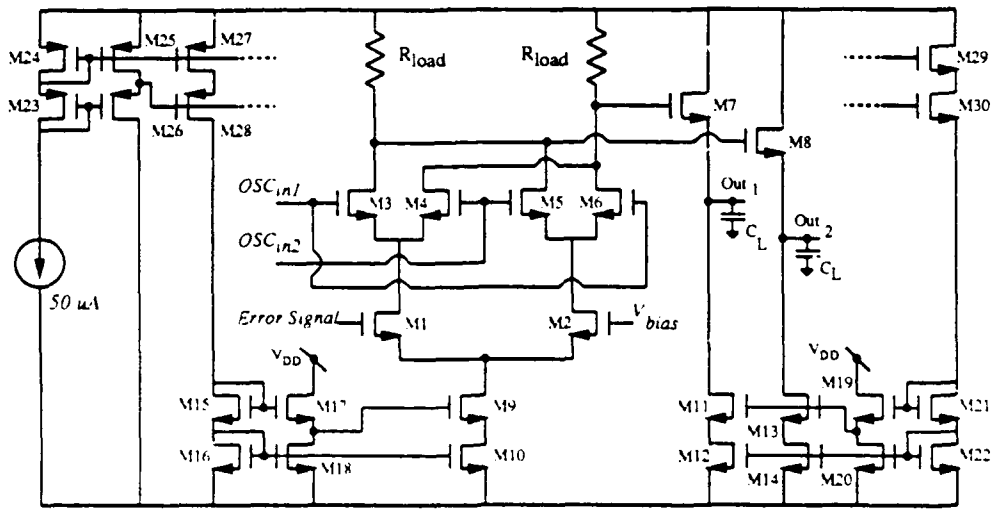
$$V_{out} = I_{bias} R_{load} = 2.5 \tag{2.63}$$

A large resistance value, R, increases the time constant associated with the resistor and the parasitic capacitance of the node, slowing the circuit operation. A large current degrades signal swing as it decreases the range that the differential pair remains in saturation. Utilizing the improved cascode current source to bias the differential pair helps to widen the biasing margin. Simulation demonstrated the best results with a current of $500\mu A$ and $5K\Omega$ resistors. With large differential devices, the modulator achieves a gain of $g_m R_L \simeq 16$.

The load resistor and output current requirement present a tradeoff situation in the sizing of the output devices. The output pads add a $5pF$ capacitance to the output pins. The resistance seen by that capacitance is

$$R_{out} = \frac{1}{g_m} = \frac{1}{\sqrt{4K' \frac{W}{L} I_D}} \tag{2.64}$$

Thus, increasing the W/L ratio will decrease the resistance and decrease the



Devices	W/L
M1-M2	400/2
M3-M6	20/2
M7-M8	240/2
M9-M10	900/2
M11-M14	640/2
M15	18/2
M16-M18	80/2
M19-M21	20/2
M22	5/2
M23	18/2
M24-M26	84/2
M27-M30	90/2

Figure 2.31: Modulator Circuit Schematic

associated time constant

$$\tau_1 = C_{Load} R_{out} \tag{2.65}$$

However, the gate capacitance of the output stage increases with size

$$C_{gs} \simeq \frac{2}{3} W L C_{ox} \tag{2.66}$$

where $C_{ox} = .86 fF/\mu^2$ for the MOSIS process. Thus, increases in size increase the time constant

$$\tau_2 = C_{gate} R_{load} \tag{2.67}$$

Equating the two time constants prevents either time constant from dominating. A sizing ratio of 240/2 results in nearly equal time constants

$$\tau_1 = 1.11 ns \tag{2.68}$$

$$\tau_2 = 1.37 ns \tag{2.69}$$

The output drivers are also biased with the improved cascode current sources to ensure that the current mirrors can sustain the high bias current and remain in saturation.

Chapter 3

Simulation

The circuit topologies presented in Chapter 2 were initially derived using rough hand calculations and first order MOSFET models. Although first order calculations provided some understanding of circuit operation, they did not provide an estimation of performance suitable for integrated circuit design. A thorough design requires higher order models and a consideration of the parasitic circuit elements associated with integrated circuits. Such analysis requires computer simulation. Furthermore, utilizing computer simulation as a design tool quickly reveals how manipulating device sizes and circuit topologies affected many different responses of the system. Thus, HSPICE, a circuit simulator, was used to further develop the basic topologies presented in chapter 2. HSPICE was produced by Meta-Software, Inc., and was implemented on a DEC VAXstation II/GPX. MOSIS provided several HSPICE models which characterized the devices produced by different vendors participating in the MOSIS program. Using the typical models in the simulator,

the rough circuit topologies were modified and adjusted to meet the design goals. The final schematics presented in Chapter 2 were developed via this iterative simulation/design process. This chapter presents the results of the simulation of these final designs.

3.1 Bandgap Voltage Reference

As previously described, the bandgap voltage reference consists of a bias network that produces a temperature independent "magic voltage" and an operational amplifier follower circuit which scales that voltage to a 1.5 volt reference voltage. Both the bias network and the operational amplifier were simulated with a 4.5 volt power supply to ensure that the bandgap voltage reference is fully operational and providing a stable reference before the power converter reaches its final output voltage. Figure 3.1 shows the simulation results of the magic voltage over a 0-70°C temperature range. This reference voltage is applied to an operational amplifier voltage follower circuit. The frequency response shown in Fig. 3.2 demonstrates that the amplifier is stable with a 60° phase margin. The operational amplifier follower circuit scales the temperature independent voltage to produce a 1.5 volt reference. The temperature dependence of the 1.5 volt reference voltage is shown in Fig. 3.3. Simulation results show a stable reference voltage of 1.5 V $\pm$ 1% over the 0-70°C temperature range.

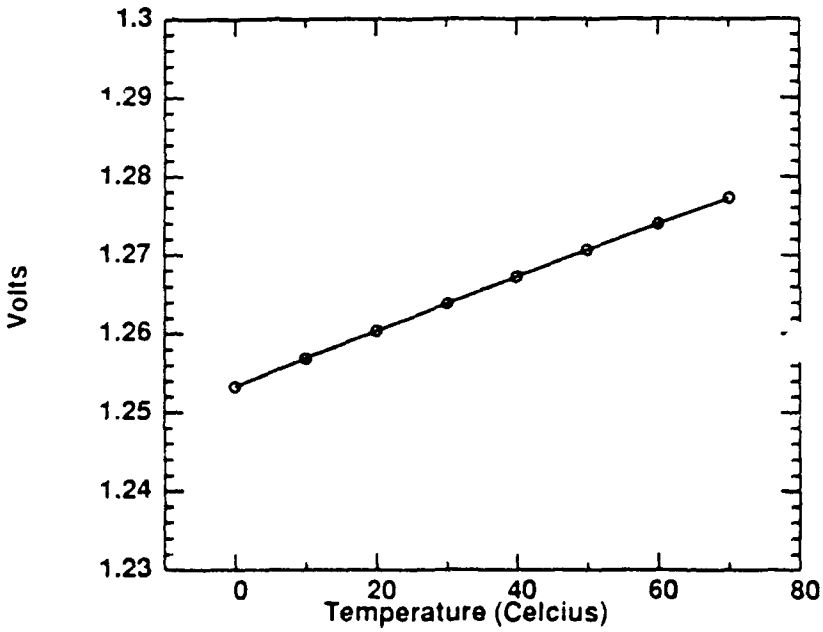


Figure 3.1. Simulated Temperature Dependence of Magic Voltage

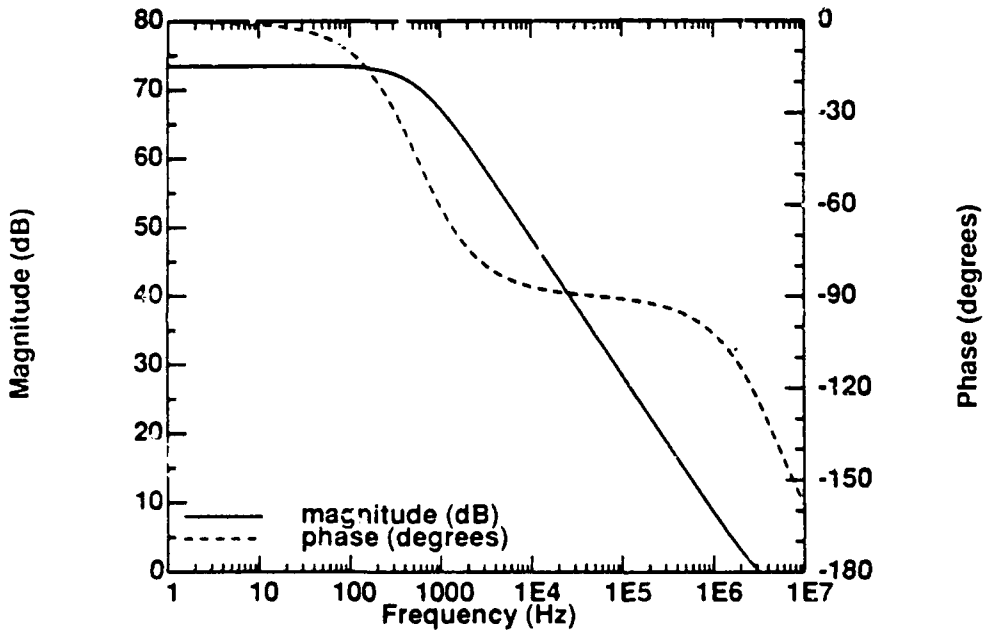


Figure 3.2: Simulated Frequency response of Operational Amplifier used in Bandgap Voltage Reference

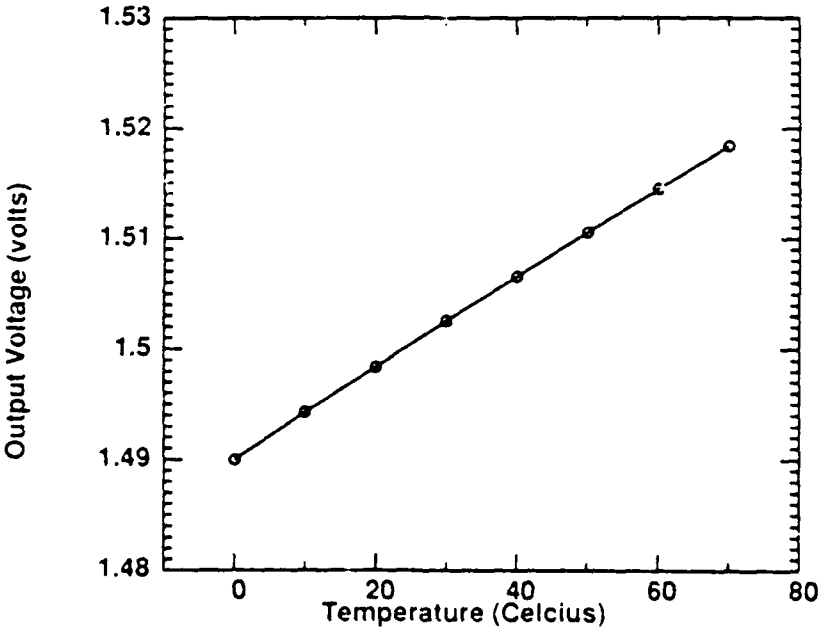


Figure 3.3. Simulated Temperature Dependence of Voltage Reference

3.2 Oscillator

The Schmitt-trigger oscillator, divider, and phase splitter drawn from Dr. Casey's library of subcells were modified to accommodate a 5 volt power supply and resimulated using HSPICE. The results closely resembled the simulations performed by Dr. Casey.

3.2.1 Schmitt-trigger Oscillator

Figure 3.4 portrays the switching levels of the Schmitt trigger component of the oscillator. The switching thresholds of 2.9 volts for the low to high transition and 2 volts for the high to low transition differed from the thresholds assumed in the rough hand calculations. However, the circuit still exhibited the Schmitt trigger behavior necessary for oscillator operation as demonstrated in the simulation results of the Schmitt-trigger oscillator shown in Fig. 3.5. The duty cycle of the square wave was unimportant because the divider circuitry triggers off the rising edge of the signal produced by the Schmitt-trigger oscillator.

3.2.2 Divider

The divider circuit incorporated an improvement over the the divider circuit used by Dr. Casey. The divider utilized a scaled NAND gate S-R latch rather than a NOR gate latch. Figure 3.7 shows the high-to-low transition of the output in response to a RESET input command. The RESET

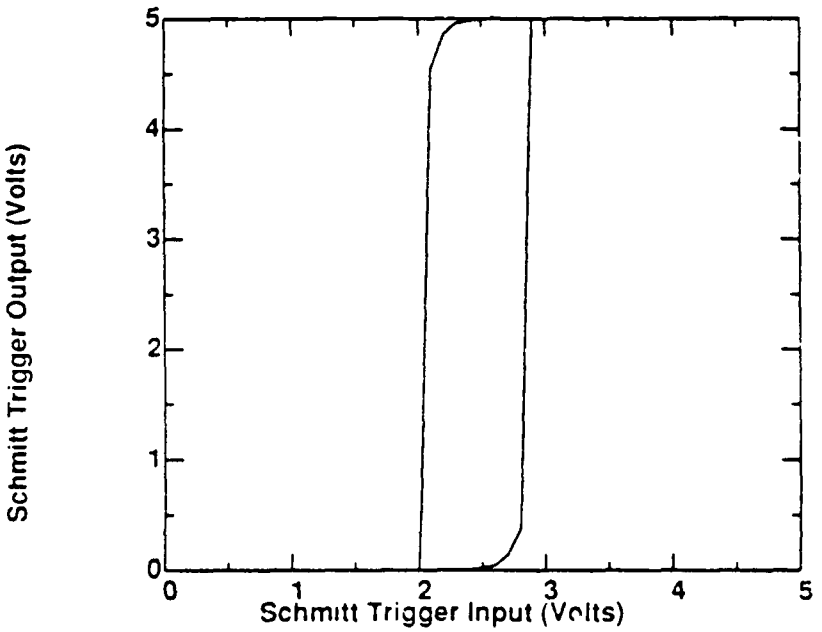


Figure 3.4 Schmitt Trigger HSPICE Simulation

transition involved two gate delays from input to output. Figure 3.6 shows the low-to-high transition of the latch output corresponding to a SET input command. The SET command activated the output with only a single gate delay. However, the gate delay was increased to match the two gate delays of the RESET command by scaling the transistor widths. The two outputs are superimposed in Fig. 3.8, displaying crossover at 2.5 volts for a 50% duty cycle.

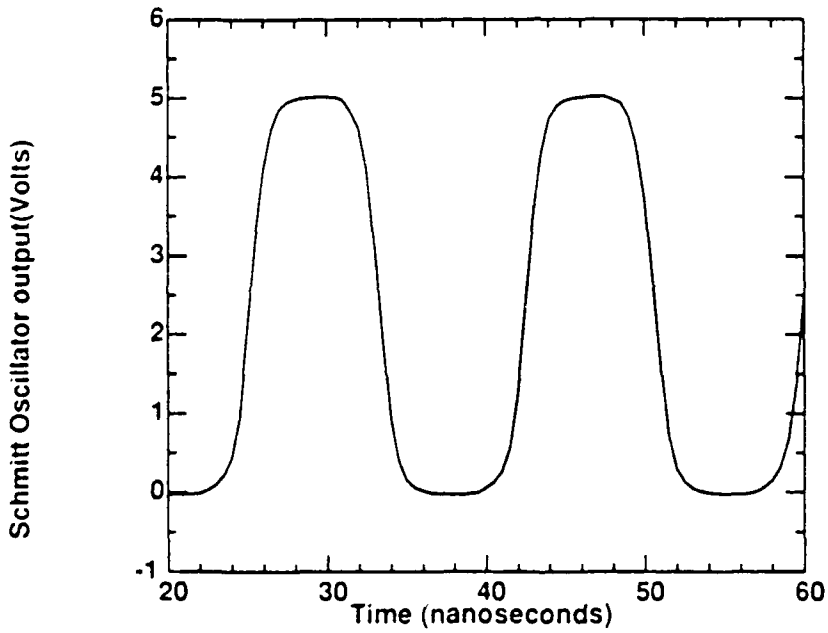


Figure 3.5: Simulated Schmitt-trigger Oscillator Output

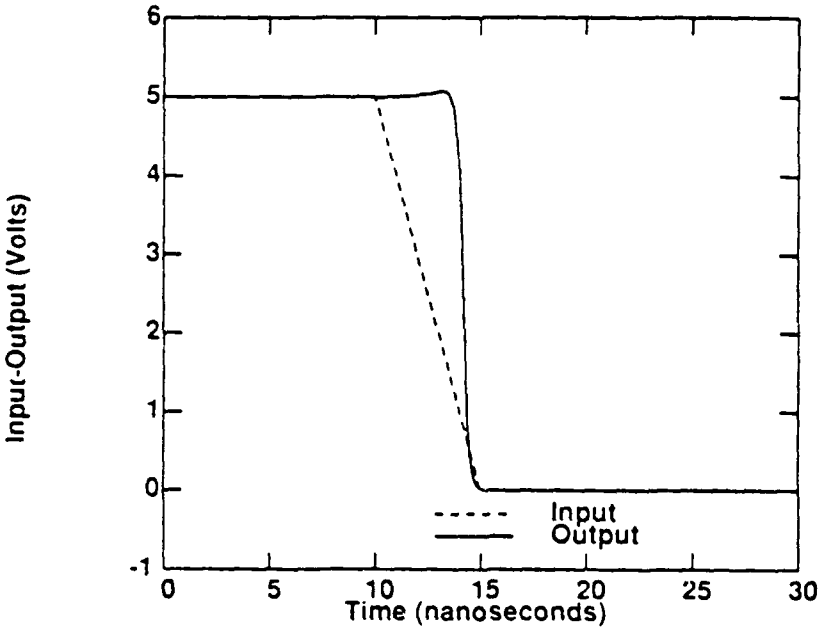


Figure 3.6 Two Gate Delay Transition

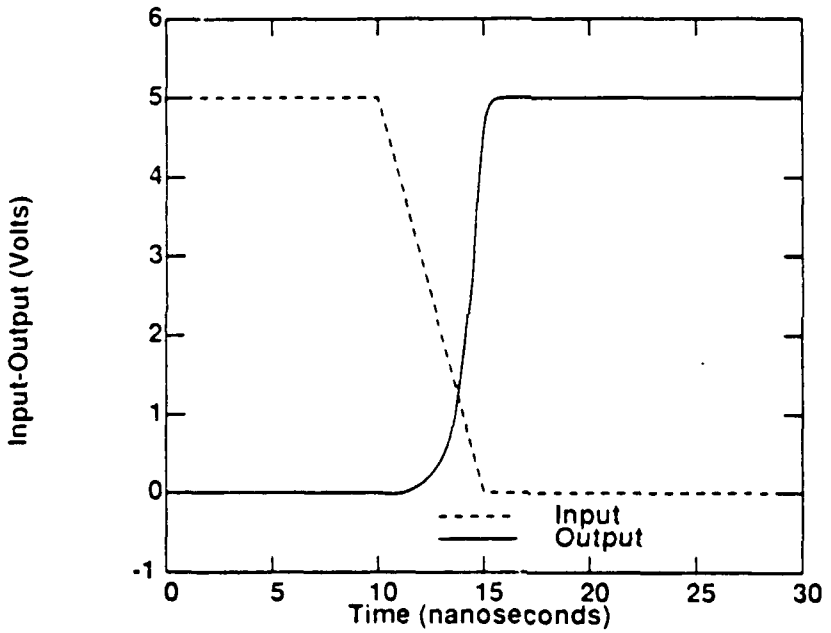


Figure 3.7. One Gate Delay Transition

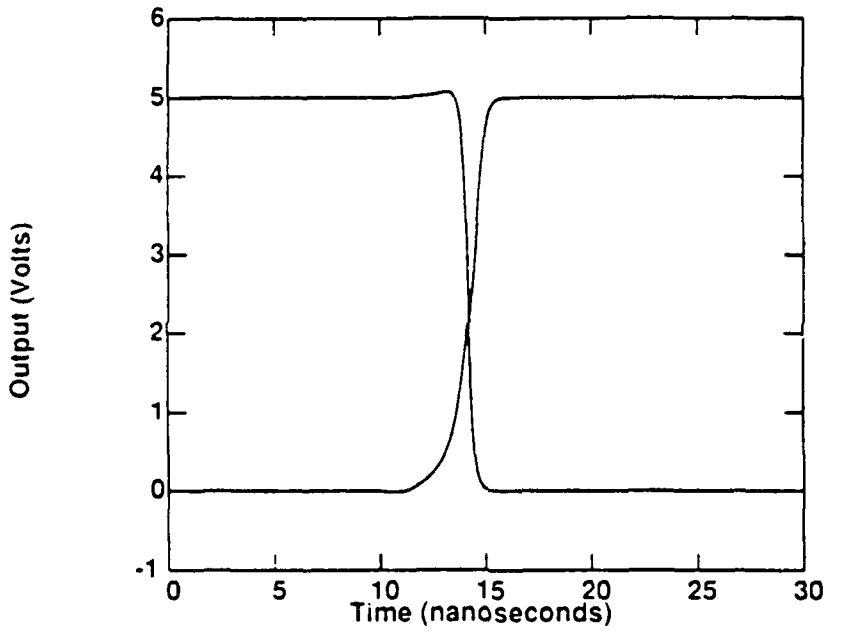


Figure 3.8 Superimposed Transitions

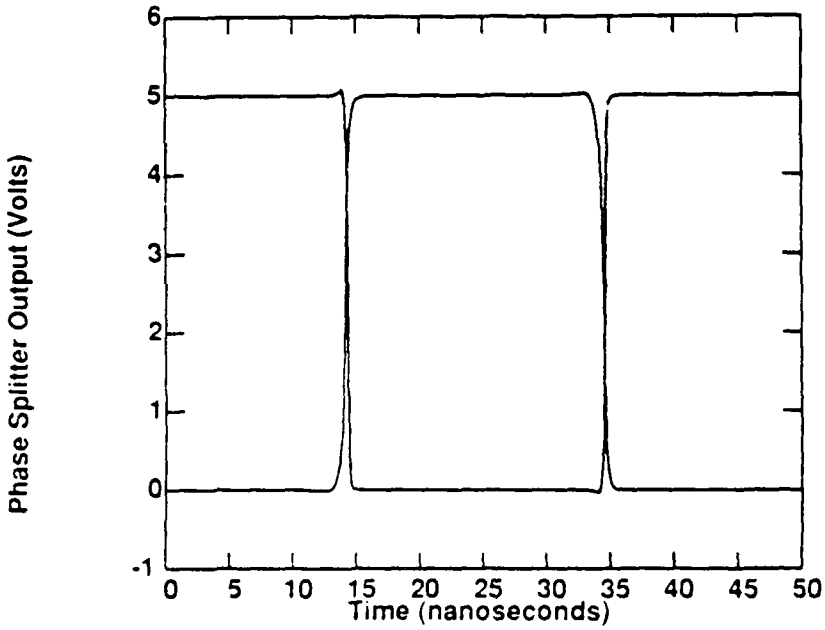


Figure 3.9. Simulated Phase Splitter Output

3.2.3 Phase Splitter

The phase splitter produced two out of phase square waves from a single square wave input. The two outputs are shown superimposed in Fig. 3.9. The simulated waveforms exhibited an acceptable delay of 0.5 ns.

3.3 Error Amplifier

The error amplifier design strove to achieve a high bandwidth with moderate DC gain, as well as high power supply and common mode rejection ratios. The small signal analysis of the amplifier resulted in a DC gain of

$$A_v = g_{m_1} R_o = (903 \frac{\mu A}{V})(2.54\ M\Omega) = 2,294 \tag{3.1}$$

The low frequency pole occurred at

$$P_1 = \left(\frac{1}{R_o C_L}\right)\left(\frac{1}{2\pi}\right) = 10\ \text{kHz} \tag{3.2}$$

resulting a unity gain crossover frequency of

$$f_c = \left(\frac{g_{m_1}}{C_L}\right)\left(\frac{1}{2\pi}\right) = 23.2\ \text{MHz} \tag{3.3}$$

Layout techniques minimized the parasitic capacitance which dominated the next significant pole, $\omega = g_{m_6}/C_p$, resulting in a phase margin of 90 degrees. The Bode diagram of Fig. 3.10 summarizes the frequency response simulation of the error amplifier.

In order to preserve the high frequency characteristics of the operational amplifier, the analog inverter required for startup needed a bandwidth that exceeded that of the error amplifier. The simulation results shown in Fig. 3.11 show how the inverter achieves unity gain inversion with a unity gain crossover frequency a decade above the operational amplifier.

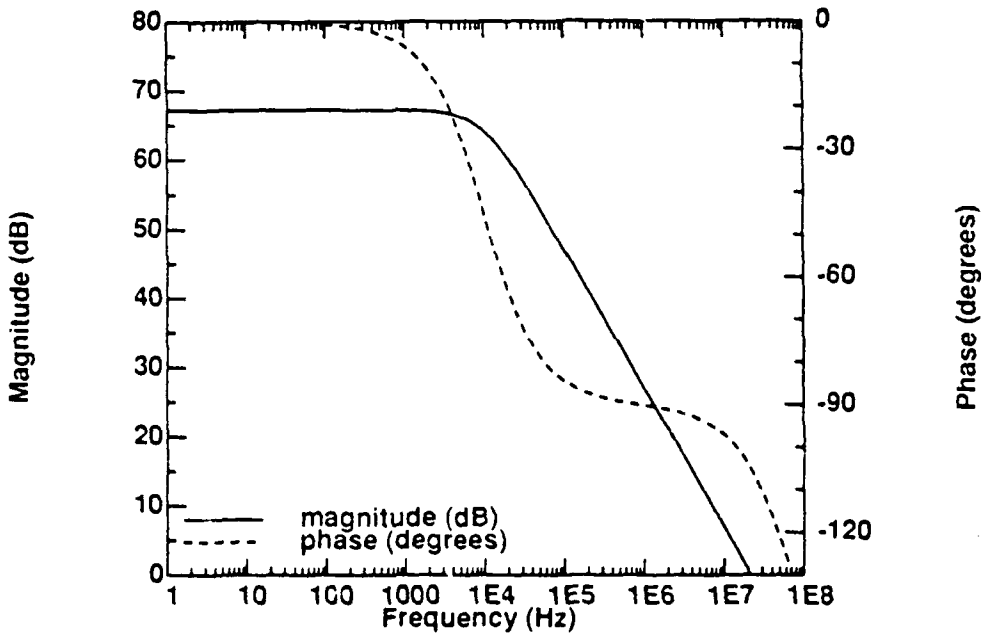


Figure 3 '0: Error Amplifier Simulated Frequency Response

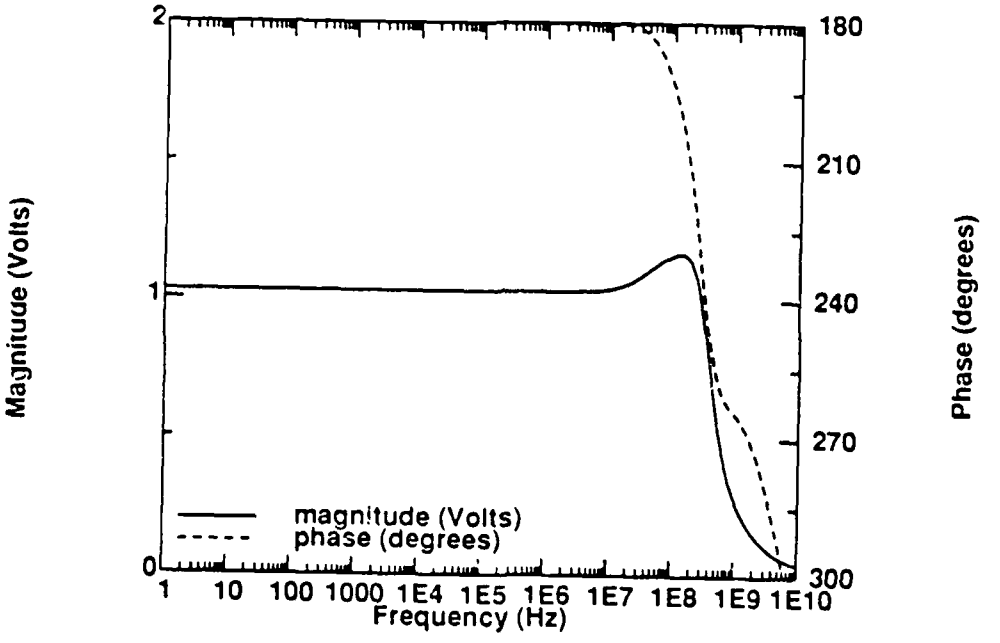


Figure 3.11: Inverter Simulated Frequency Response

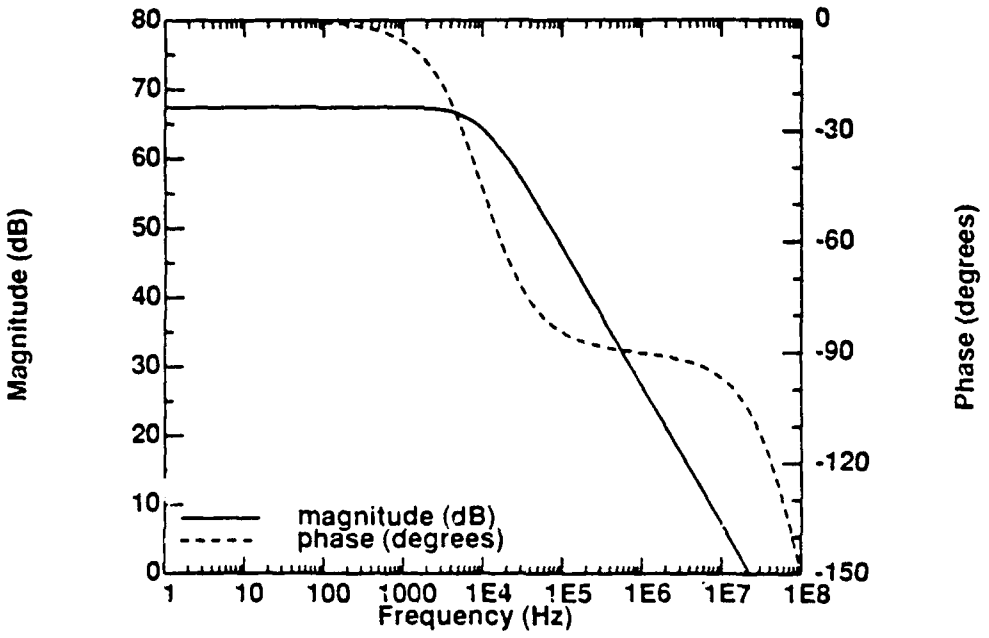


Figure 3.12: Simulated Frequency Response of Cascaded Operational Amplifier and Inverter

Cascading the inverter and operational amplifier produced the frequency response shown in Fig. 3.12. The operational amplifier limited the bandwidth while the inverter decreased the phase margin by 30 degrees.

Figure 3.13 shows the power supply rejection ratio of the error amplifier as a function of frequency. The power supply rejection ratio is defined as [11]

$$PSRR = \frac{A_D}{A_P} \tag{3.4}$$

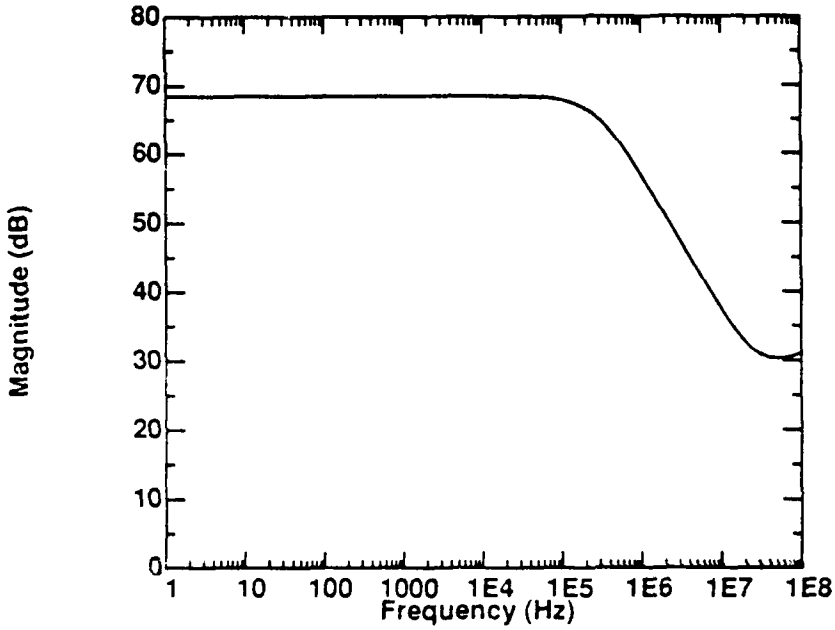


Figure 3.13: Simulated Power Supply Rejection Ratio

where A_D is the amplifiers differential gain and A_P is the ratio of the response at the amplifier output to a signal on the power supply rail. Thus the PSRR of the error amplifier decreases with frequency as shown in Fig. 3.13

The remaining simulation results of the error amplifier are summarized in Table 3.1.

Parameter	Test Condition		units
Input Offset Voltage	$V_{cm} = 1.5V$	0.238	mV
Input Bias Current	$V_{cm} = 1.5V$	0	μA
Input Offset Current	$V_{cm} = 1.5V$	0	μA
Small Signal Open Loop Gain		68	dB
CMRR	V_{cm} 1 - 3.5 V	98	dB
PSRR	DC	69	dB
Output Swing		1.5	V
Max Sink Current		500	μA
Max Source Current		5	mA
Unity Gain Bandwidth		23	MHz

Table 3.1: Error Amplifier Simulation Results

3.4 Modulator

The complete simulation of the modulator combined all of the feedback generator elements. The error amplifier input to the modulator was a 0.4 V_{p-p}, 1 MHz sine wave. The 20 MHz carrier wave was supplied from the phase splitter outputs. The modulator outputs were driving 5 pF load capacitances to simulate the capacitance of the IC bonding pad. Figure 3.14 shows the simulation results of the modulator output.

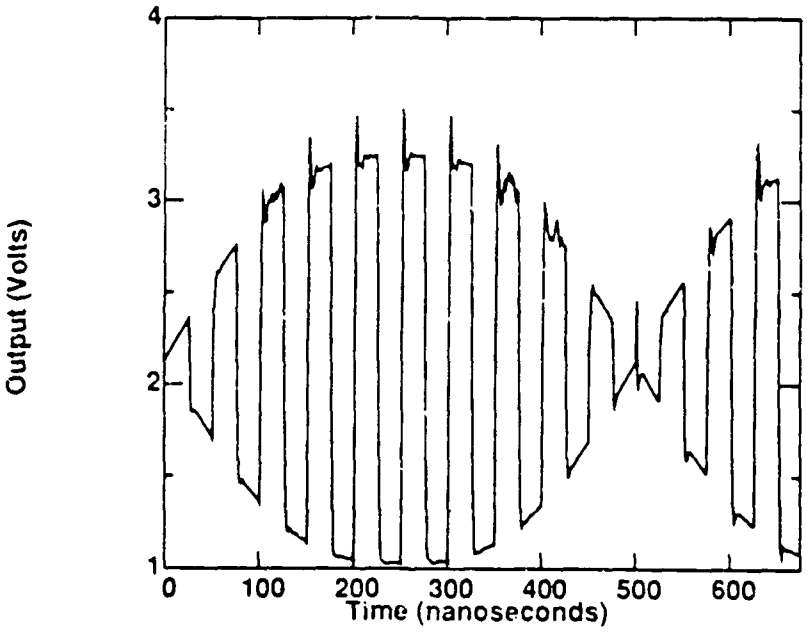


Figure 3.14: Simulated Modulator Output

Chapter 4

Layout

Before the feedback controller circuitry could be submitted to MOSIS for fabrication, the physical arrangement and implementation of the circuit elements had to be defined by means of an integrated circuit layout. Although this chapter addresses the layout separately, layout considerations were an integral part of the design/simulation process. In addition to modeling the device parameters of typical MOSIS fabrication facilities, HSPICE also simulated the effects of different layout geometries and device placement. This chapter addresses layout-dependent aspects of circuit performance. Translating the simulated circuits into an integrated circuit mask also involved adapting several features of the MOSIS fabrication process. The MOSIS process is tailored to accommodate CMOS digital logic circuits. This chapter discusses the adaptations required to utilize the MOSIS facility for analog integrated circuit design. Finally, the fabricated circuits received from MOSIS contained a layout error which was repaired using an innovative application

of a Focused Ion Beam (FIB). Repair work on the feedback controller IC demonstrated the suitability of the FIB for both detaching and connecting metal lines on integrated circuits.

4.1 Circuit Performance

4.1.1 Body Effect

In the MOSIS n-well process, the n-channel transistors are fabricated directly on the p-type substrate, while the p-channel devices are placed in n-type wells. The bulk (or well) substrate voltage directly impacts the threshold voltage of the MOSFET. The threshold voltage is defined as [8]

$$V_t = V_{to} + \gamma(V_{SB})^{1/2} \tag{4.1}$$

where V_{SB} is the source to bulk voltage, V_{to} is the zero bias threshold voltage and γ is a constant which depends upon processing parameters such as the doping concentrations and the oxide thickness. Typically, $\gamma = 0.5$ for MOSIS fabrication processes.

The increased threshold voltage due to the body effect greatly impacts the biasing of the bandgap reference circuit shown in Fig. 4.1. The body effect increases the threshold voltages of M1-M8 which increases the required rail voltage necessary to bias the current mirrors. However, the body effect for the p-devices M5-M8 was eliminated by placing those devices in separate wells and tying the source of each transistor to the well.

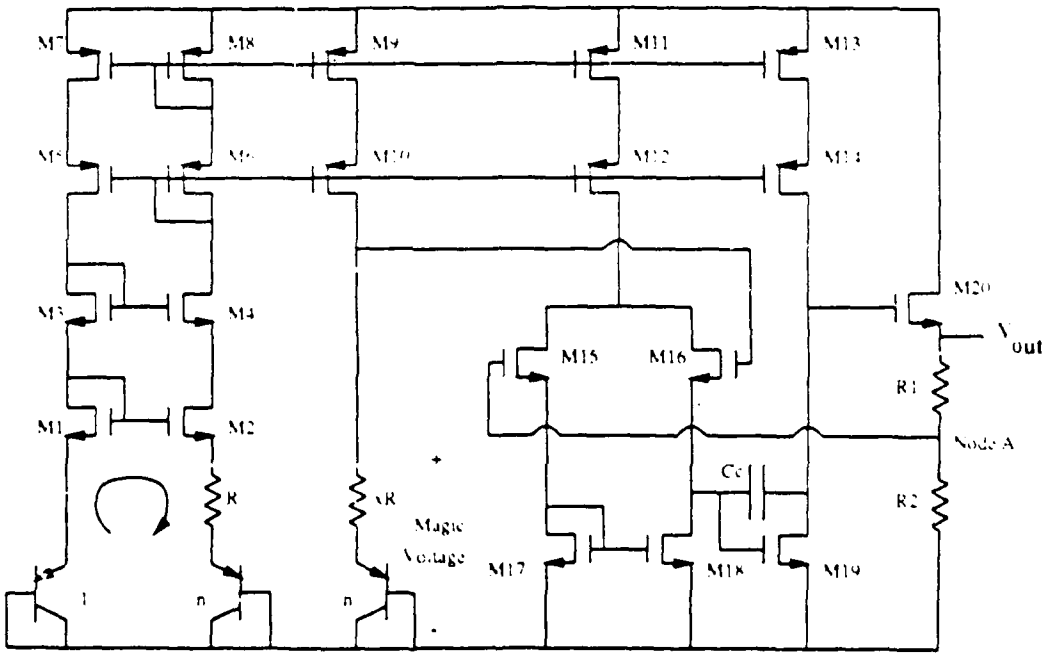


Figure 4.1 Bandgap Reference Circuit

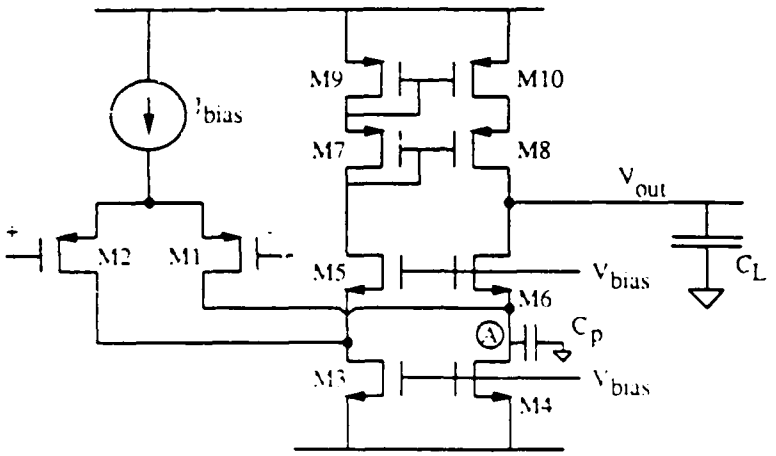
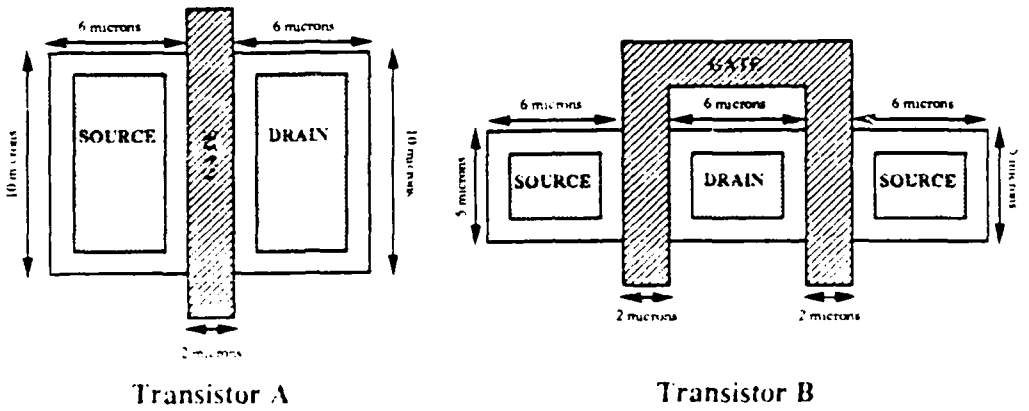


Figure 4.2: Error Amplifier Circuit

4.1.2 Parasitic Capacitances

The MOSFET source and drain diffusions give rise to junction-depletion capacitances which directly impact performance. As was shown in Section 2.4.2, the second dominant pole of the error amplifier is determined by g_{ms}/C_p, where C_p is the parasitic capacitance of Node A, as shown in Fig. 4.2. Increasing the bandwidth of the amplifier equates to pushing the secondary pole out to higher frequencies. Thus, the drain-to-bulk parasitic capacitance of transistors M1 and M4, and the source-to-bulk parasitic capacitance of transistor M6, decrease the bandwidth of the amplifier. A transistor-folding layout technique can decrease the parasitic junction-depletion capacitance without decreasing the W/L ratios of the devices.

The source and drain diffusion areas form a p-n junction with the sub-



Transistor A Transistor B

Figure 4.3 Minimizing Drain Capacitance (W/L = 10/2)

strate. The sides of the diffusion and the bottom area of the diffusion all contribute to the parasitic junction capacitance. Thus the capacitance to the substrate for the drain is

$$C_d = C_j(Area\ of\ bottom) + C_{jsw}(Perimeter) \tag{4.2}$$

where C_j is the drain-bulk junction capacitance and C_{jsw} is the side-wall periphery capacitance. Typical MOSIS parameters are

$$C_j = 0.29\ fF/\mu m^2 \tag{4.3}$$

$$C_{jsw} = 0.34\ fF/\mu m \tag{4.4}$$

Thus, to minimize parasitic capacitances the layout should minimize drain or source perimeter and area. Figure 4.3 shows two transistors, both with

W/L ratios of 10/2. Transistor A has a drain and source area of 60 μm^2 and a perimeter of 22 μm. Transistor B has a source area of 60 μm^2 and a source perimeter of 34 μm. However, the drain of Transistor B has an area of 30 μm^2 and a perimeter of 12 μm. Thus the drain-to-bulk capacitance of Transistor B is approximately half that of Transistor A. Although the source-to-bulk capacitance is significantly higher, the added capacitance is placed where it is unimportant to the circuit. For instance, in the error amplifier, if the drain capacitance of transistor M4 is minimized, the source capacitance is increased. However, additional source capacitance only adds capacitance to the ground node where it will not affect circuit performance. Similarly, minimizing the source capacitance of transistor M6 significantly increases the drain capacitance. But, such an increase only adds capacitance to the output node where it simply adds to the compensation capacitor. The same arrangement applies to the input differential pair as well. Throughout the layout, capacitance was minimized on critical nodes and shifted to unimportant nodes by proper folding of the devices.

4.2 Circuit Elements

The circuits presented in Chapter 2 were implemented in the MOSIS 2-micron, n-well process. The manufacturing process was designed to accommodate CMOS digital logic circuits. Therefore, several circuit elements required for analog circuit design, namely bipolar transistors, capacitors, and

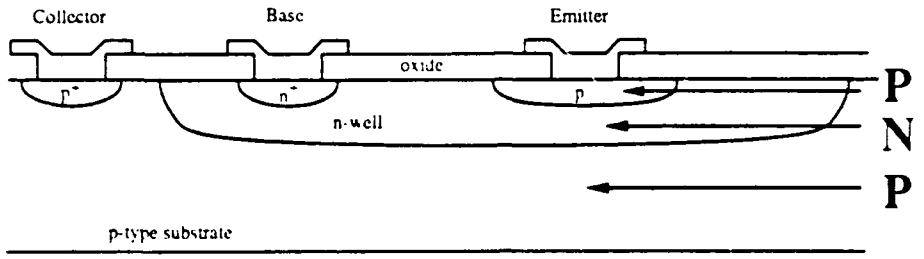


Figure 4.4: Cross-Sectional View of Parasitic Bipolar Transistor

resistors, were developed from the available mask layers.

4.2.1 Bipolar Transistors

The bandgap reference circuit shown in Fig. 4.1 required bipolar transistors with area ratios scaled 1:49. Although the CMOS process offered by MOSIS does not provide bipolar devices, the technology contains an inherent p-n-p transistor. A p-diffusion in an n-well in the p-substrate produces a parasitic p-n-p structure, as shown in Fig. 4.4. A single emitter diffusion of 10μm x 10μm was utilized for the unity size transistor. The scaled transistor was implemented with forty-nine 10μm x 10μm emitters diffused into a single well. The two bipolar structures are shown in Fig. 4.5. The well contacts around the edge of the emitter array formed the base contact and the substrate contacts around the edges of the well provided the collector contact.

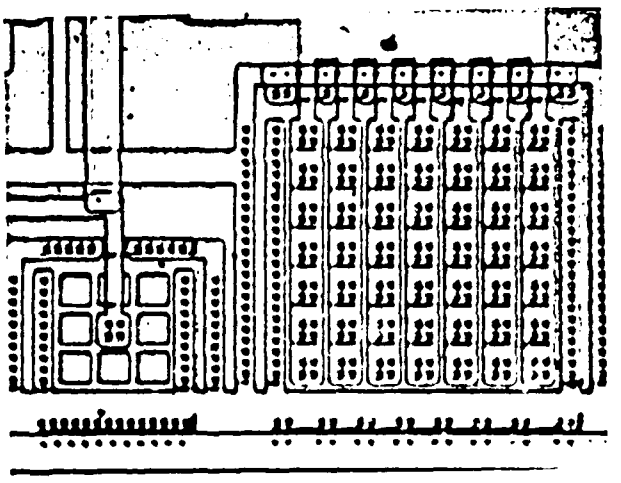


Figure 4.5. Scaled Bipolar Transistors

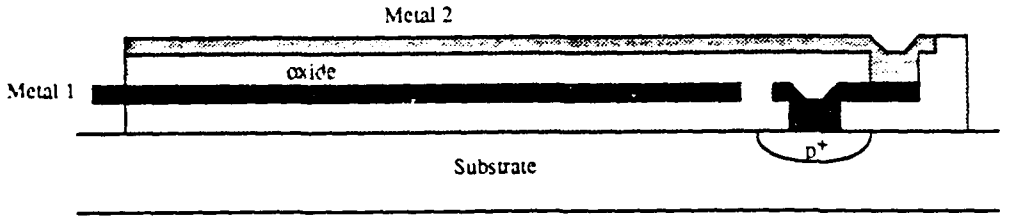


Figure 4.6: Cross-Sectional View of Capacitor Sandwich

4.2.2 Capacitors

The error amplifier and the operational amplifier in the bandgap reference circuit required compensation capacitors to insure stability. The current source in the oscillator circuit charged and discharged a capacitor to trigger the Schmitt trigger. These capacitors were fabricated by utilizing parasitic capacitances inherent in the MOSIS process. The capacitance between the two metal layers was approximately $0.049 fF/\mu m^2$ while the capacitance between metal 1 and the substrate or well was approximately $0.026 fF/\mu m^2$. Sandwiching a metal 1 layer between a metal 2 layer and the substrate created a structure that had a capacitance of approximately $0.075 fF/\mu m^2$. Figure 4.6 depicts the capacitor sandwich structure. Thus, the error amplifier's 6 pF compensation capacitor required a capacitor structure of approximately 285μm x 285μm. When one terminal of the capacitor is grounded, the substrate forms the bottom plate of the capacitor. When neither terminals are grounded, an n-well forms the bottom layer.

After the circuitry presented in this thesis was fabricated, MOSIS offered

a new double-poly process. Using this new process, capacitors can be easily fabricated by overlapping the two layers of polysilicon. The polysilicon capacitors also provide a much higher capacitance per unit area.

4.2.3 Resistors

The resistors were implemented in polysilicon. Typical values of polysilicon sheet resistance vary from 20–40 ohms/square, depending on the particular vendor performing the fabrication for MOSIS. Thus, whenever possible, circuits were designed to operate on resistor ratios, not absolute values. For instance, in the bandgap circuit shown in Fig. 4.1, the temperature independent voltage is dependent upon the ratio of resistors, x, not the particular resistor values. To facilitate matching in the resistor ratios, the smaller resistor was laid out in a reproducible geometric shape and the larger resistor consisted of multiples of that shape. In addition, a binary-weighted resistor trimming ladder was added to the end of each resistor. Before trimming, metal 2 shorts out the entire trimming ladder. The metal 2 lines formed jumper wires that can be broken with a probe to add binary-weighted increments of resistance to the existing resistor. For instance, to add an additional 20 squares of resistance, the jumpers shorting out sections of 16 and 4 squares can be removed. However, in some instances, particularly the modulator, an absolute resistance value is desired. In this case, the resistor layout assumes a typical value of 23 ohms/square with a large enough trimming structure to accommodate resistance variations of 20-40 ohms/square. Figure 4.7 shows

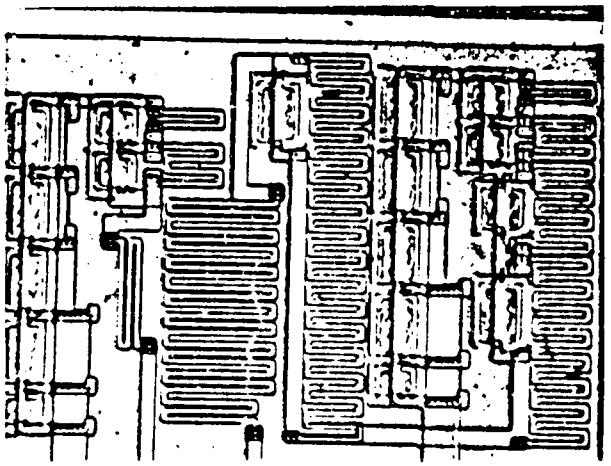


Figure 4.7: Trimmable Polysilicon Resistor Structures

two ratioed polysilicon resistors and their binary weighted trimming ladders.

4.3 Focused Ion Beam Circuit Repair

The original mask submitted to MOSIS contained a layout error in the bandgap reference circuit. Specifically, the collector, base, and emitter of the single emitter or unity-sized bipolar transistor were shorted to ground, rendering the circuit inoperable. As shown in the bandgap schematic in Fig. 4.1, the base and collector of the diode-connected transistor were connected to ground. However, the layout error also shorted the emitter t

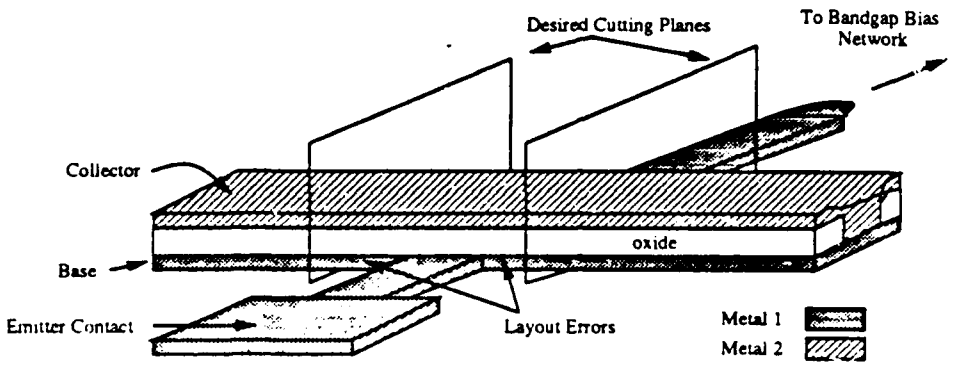


Figure 4.8: Layout error in the Bipolar Transistor repaired with Focused Ion Beam Cutting

ground. Figure 4.8 depicts the layout error. A metal 1 layer connected the emitter contact to the rest of the bandgap circuitry. However, the metal 1 base lead crossed the emitter lead, shorting together the emitter, base, and collector. Fortunately, the base and collector terminals were connected to ground via other connections on both sides of the emitter lead. Thus, the circuit could be repaired by making two cuts, one on either side of the emitter lead as shown in Fig. 4.8

The microsurgery was performed at MIT by Tao Tao using the SIM 50 Focused Ion Beam. The SIM 50 utilizes Gallium for its liquid metal ion source. The operating conditions during the milling are shown in Table 4.1. Figure 4.9 shows the area before and after the milling. Before the cutting, the device exhibited short-circuit characteristics. After the cutting, the diode

Operating Conditions	
Gallium ion energy	30 keV
Ion Current	140–240 pA
Milling Time	30 min.
Ion Beam scan rate	3.7 kHz

Table 4.1: Focused Ion Beam Milling Conditions

connected transistor exhibited the typical diode $I-V$ characteristics as shown in Fig. 4.10. The apparent low breakdown voltage for negative voltages is due to the substrate-source p-n junction of transistor M1 of the bandgap circuit. This substrate-source diode turns on when the test voltage falls less than -0.6 volts. However, the forward bias condition demonstrates the success of the FIB repair.

The success of the FIB cutting operation led to further investigation of integrated circuit repair. The focused ion beam is capable of metal deposition as well as milling. Previous work had demonstrated the feasibility of connecting two levels of metal at an intersection [12] . This work was repeated, connecting two crossing aluminum lines by milling a hole through both lines and depositing platinum into the hole. The connection had a resistance of 5 Ω and withstood a maximum current of 100 mA. The deposition demonstrated the Focused Ion Beam's capability of connection as well as cutting in integrated circuit repair. However, layout repairs do not always involve connection of overlapping metal layers. Often metal lines of the same level need connecting. Thus, another application was pursued using samples

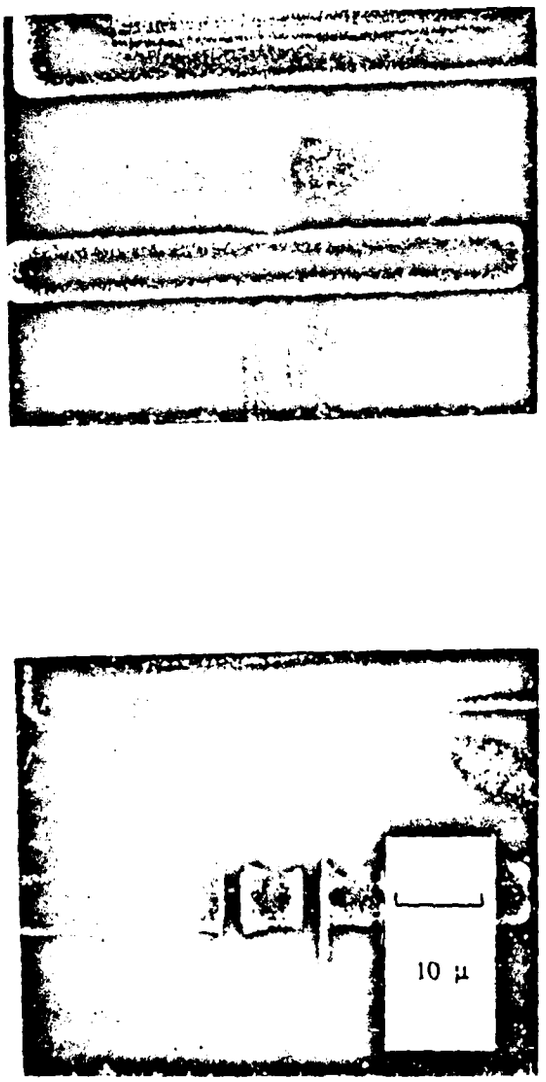


Figure 4.9: Bipolar Transistor before (top) and after (bottom) FIB repair

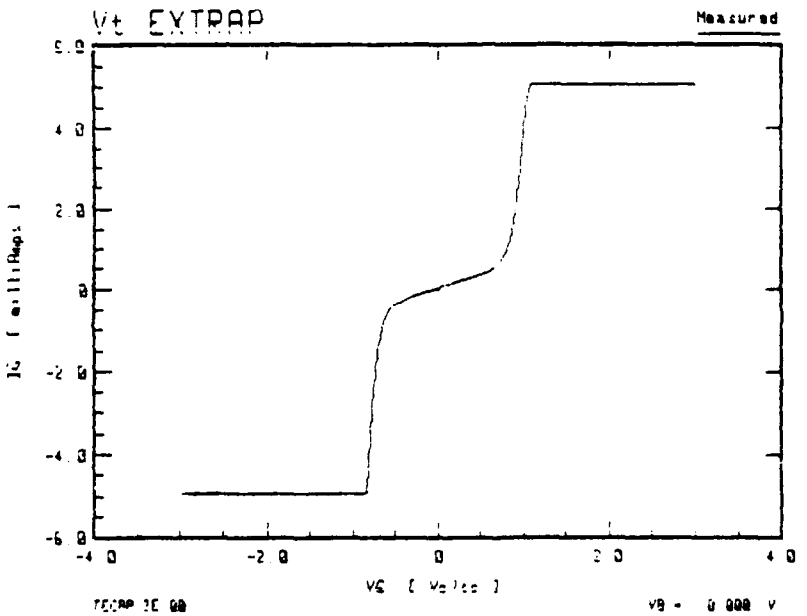


Figure 4.10: I-V characteristics of Diode-connected Transistor after FIB repair

of the feedback controller IC. The third application considered connecting parallel metal lines with a jumper wire of deposited platinum. The connection is shown in Fig. 4.11. Two parallel metal lines, 10 μm apart, were connected by a FIB-deposited jumper wire. First the FIB was used to mill a 4 μm x 4 μm hole through the protective nitride layer and into each metal line. The milling was accomplished with a Gallium ion current of 0.10 nA, cutting for ten minutes. Then platinum was deposited with an ion current of 60 pA over a 30 μm x 10 μm area, overlapping the holes. The resistance of the connection was characterized to be 300 Ω, as shown in Fig. 4.12. The thickness of the platinum film is less than 100 angstroms. Lower resistance may be achieved by using a longer deposition time, or increasing the deposition rate with higher Gallium ion current.

Although the resistance of the platinum jumper was high compared to the resistance of a metal line, such a connection has many applications in CMOS integrated circuits. The high resistance is undesirable for high speed signal lines, but is well suited for biasing gates of transistors, in a current mirror for example, where there is no appreciable current flow. The cutting, connection of intersecting lines, and jumper wire deposition demonstrated the viability of the focused ion beam as an integrated circuit repair tool. FIB repair provides a quicker, significantly less expensive method of repairing a defective prototype IC rather than refabricating an entirely new device.

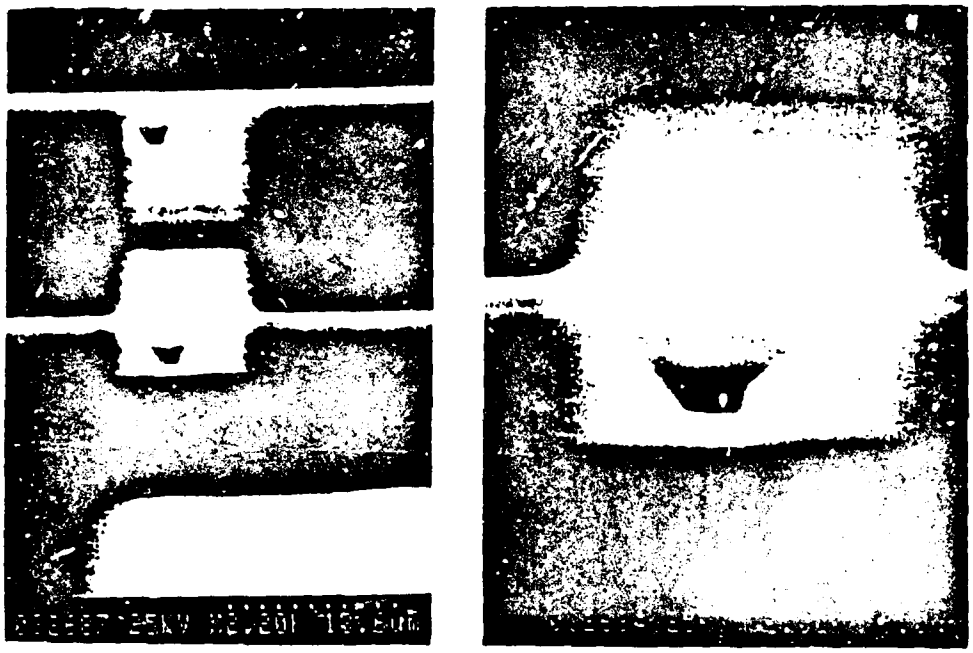


Figure 4.11: Platinum Jumper Interconnect of two Parallel Aluminum lines

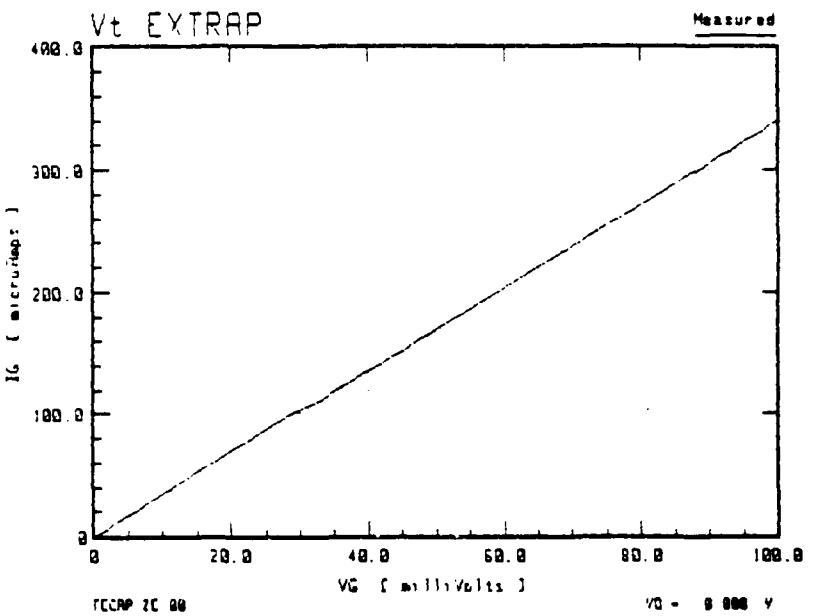


Figure 4.12: I-V characteristics of Jumper Connection

Chapter 5

Testing

In order to insure functionality and to aid in troubleshooting, the subsections of the feedback controller int ₒrated circuit were laid out and fabricated as separate entities with appropriate inputs and outputs connected directly to external pins. Such an arrangement facilitated testing of individual circuit blocks for functionality. However, connecting internal nodes to external pins sometimes diminished performance.

5.1 Bandgap Voltage Reference

The testing of the bandgap reference circuit clearly demonstrated the importance of properly balancing the competing temperature dependent components of the system. The bandgap reference circuit was thermally tested in both a Hotpack Digimatic oven and a conventional freezer. The circuit temperature was monitored with a thermocouple. The integrated circuit packages received from MOSIS had a removable cover which allowed access

to the circuit die. The thermocouple was inserted under the cover to monitor the temperature of the die. The temperature was stabilized every five degrees for measurements.

The bandgap circuit consisted of two parts, a bias network that produced a temperature independent "magic voltage," and a follower circuit that scaled the magic voltage to a 1.5 volt output voltage. Both the magic voltage and the output voltage were monitored over the temperature range. The magic voltage was governed by

$$V_{out} = V_{BE} + x\,(\ln n) V_T \tag{5.1}$$

where n was the size ratio between the two bipolar devices, and x was a ratio of resistors. In Eq. 5.1, V_{BE} exhibits a negative temperature coefficient and V_T exhibits a positive temperature coefficient. Canceling the two slopes results in temperature independence.

The parameter n was fixed at 49 by the layout geometry of the bipolar devices. However, the trimmable resistor pattern allowed modification of the parameter x. The effect of moderating x was clearly demonstrated in testing. Figure 5.1 shows the strong positive temperature coefficient of the untrimmed bandgap circuit. This circuit was tested as delivered from MOSIS. For the untrimmed circuit, $x = 7.69$, which closely approximated the simulated value of $x = 7.85$, but did not provide the desired temperature independence. Clearly, V_T dominated the magic voltage, yielding a positive temperature coefficient. Over 40°C the untrimmed output voltage was 1.885 $V \pm 1.5\%$.

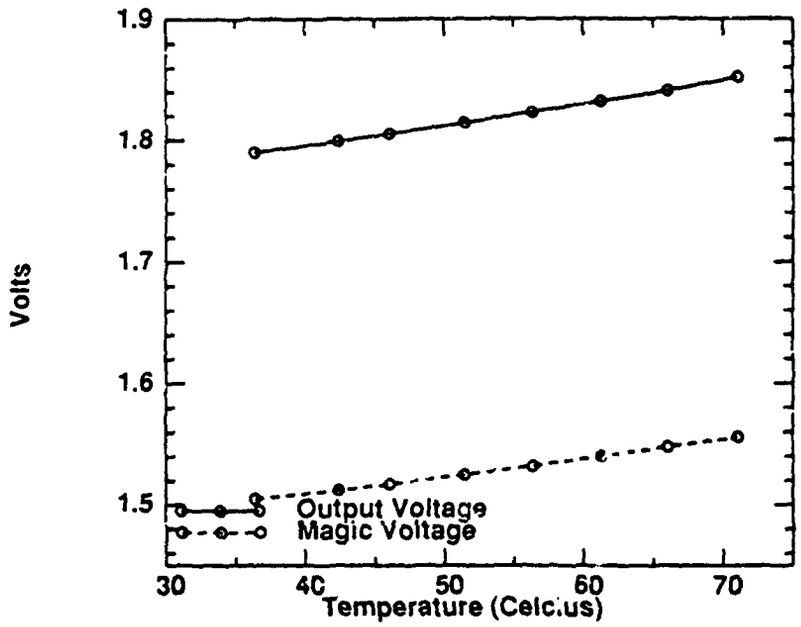


Figure 5.1: Experimental Temperature Dependence of Untrimmed Bandgap Circuit

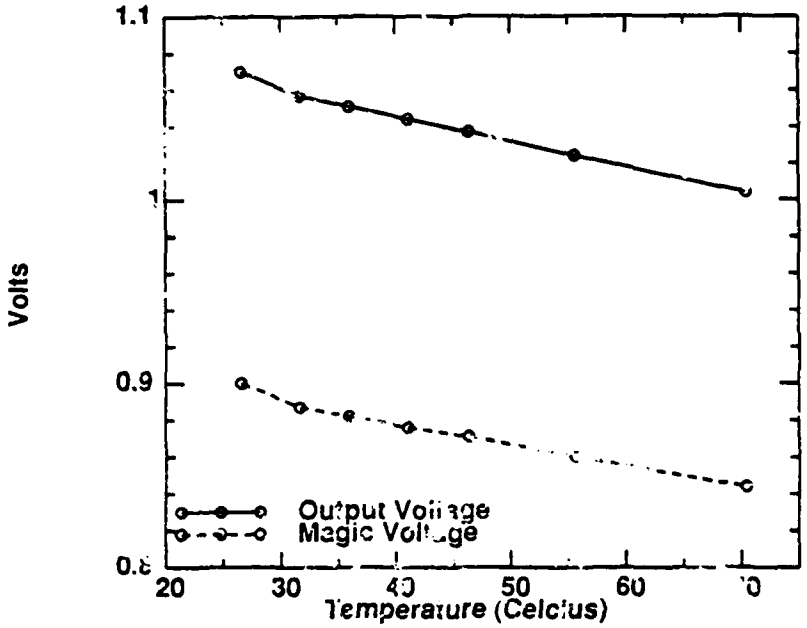


Figure 5.2: Experimental Temperature Dependence of Bandgap Circuit with x Trimmed to 2.56

Figure 5.2 shows the temperature dependence of the bandgap circuit with the value of x trimmed too low. The circuit that produced the data in Fig. 5.2 had an x of approximately 2.56. In this circuit, the negative temperature dependence of V_{BE} dominated, giving an overall negative temperature coefficient. The magic voltage was well below the desired 1.262 volts, and over a 45°C temperature range, the output voltage was 1.037 $V \pm 3.2\%$.

Finally, the value of x was adjusted to acquire a magic voltage of 1.262

volts. Although the temperature response improved greatly over the untrimmed and overtrimmed circuits, the circuit still exhibited a slight positive temperature coefficient, as did the simulations. Trimming the resistors to produce $x = 5.55$, resulted in a magic voltage of 1.193 which varied only three millivolts over 70°C as shown in Fig. 5.3. The output voltage was 1.425 $V \pm .2\%$ over the same 0-70°C range.

The bandgap reference circuit was initially designed to operate over the commercial temperature range of 0-70°C. However, when the temperature range was extended to include the upper military temperature classification of 125°C, the magic voltage varied only 27 millivolts over the extended temperature range as shown in Fig. 5.4. The output voltage was 1.425 $V \pm 1.1\%$ over the 0-125°C range. Test facilities were not available to test the bandgap circuit over the full military range of -55 to 125°C . However, based on the flatness of the low temperature response, the slope over the untested -55 to 0°C is anticipated to mirror that of the high temperature response, yielding an error of no more than $\pm 2\%$ over the full military temperature range.

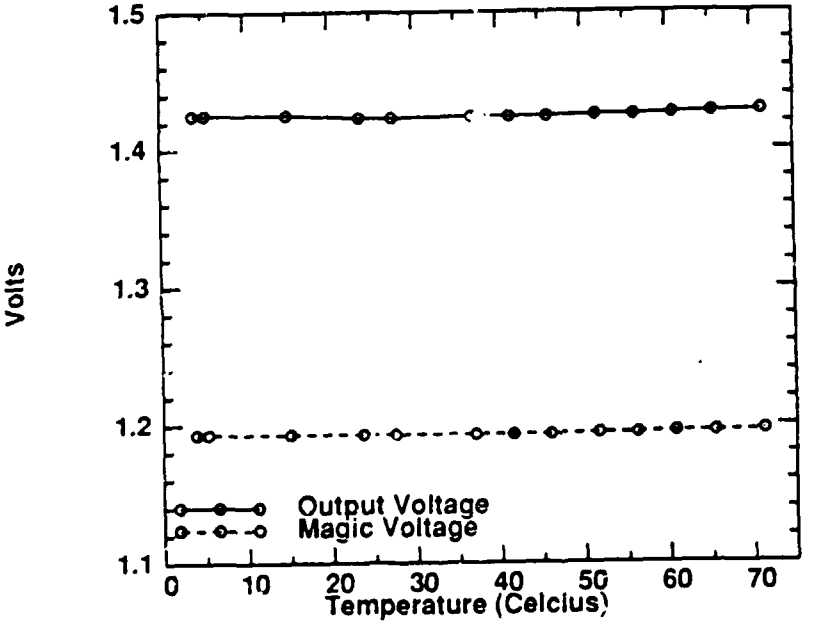


Figure 5.3: Experimental Temperature Dependence of Bandgap Circuit trimmed to 1.193 Magic Voltage

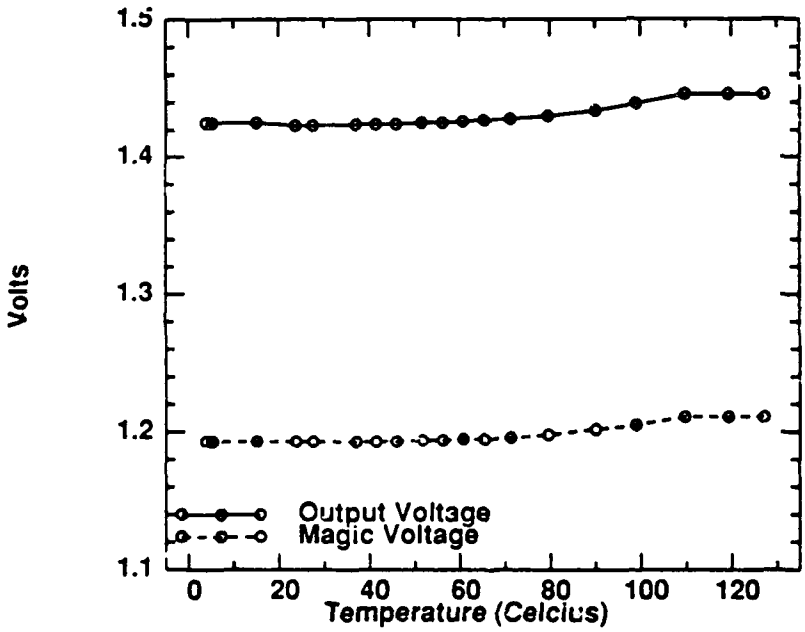


Figure 5.4: Experimental Temperature Dependence of Bandgap Circuit over Expanded Temperature Range

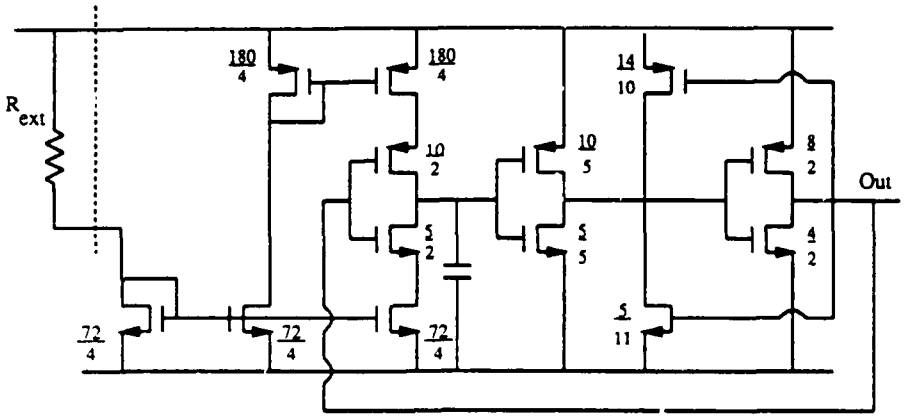


Figure 5.5: Schmitt-trigger Oscillator Circuit

5.2 Oscillator

For initial fabrication and testing, the oscillator circuit was broken down into its three main subsections, the Schmitt-trigger oscillator, the divider, and the phase splitter. The inputs and outputs of each stage were routed to external pins.

In the initial design of the Schmitt-trigger oscillator, an external 33 $k\Omega$ resistor biased a 100 μA current source which charged and discharged an on-chip capacitor. The capacitor voltage was input to a Schmitt trigger circuit whose output then fed back to control the charging and discharging of the capacitor. Figure 5.5 shows the experimental circuit. A 33 $k\Omega$ bias resistor resulted in an output square wave of 22.7 MHz as shown in Fig. 5.6.

Both hand calculations and simulations predicted an oscillator frequency of 40 MHz with a 33 $k\Omega$ bias resistor. The demonstrated performance and less than optimum wave shape can be attributed to the added capacitance of the bonding pad, external pin, and oscilloscope probe. The Schmitt-trigger oscillator was designed to drive the divider stage, an output load of three minimum-size CMOS gates. The bonding pad, pin, and oscilloscope probe add 25 pF of capacitance to the output node which is driven by minimum size transistors. Thus, after the Schmitt trigger is activated, the output inverter stage must charge or discharge the large output capacitance before the output voltage can change.

The consequences of this added capacitance can be appreciated by considering an example. When the output of the Schmitt trigger is low, the top current source is charging up the internal capacitor. When the voltage on the internal capacitor exceeds the upper threshold of the Schmitt trigger, the output n-device turns off and the output p-device turns on. The added load capacitance slows the low to high transition of the output. Meanwhile, the current source is still charging up the internal capacitor. The slow output swing gets magnified as the internal capacitor voltage overshoots the Schmitt trigger threshold. Thus, when the output finally does reach a high value, the current source has a much greater voltage to discharge as depicted in Fig. 5.7 The resulting longer discharge time equates to a slower oscillation frequency, as was observed. Thus, the test circuit demonstrated the functionality of

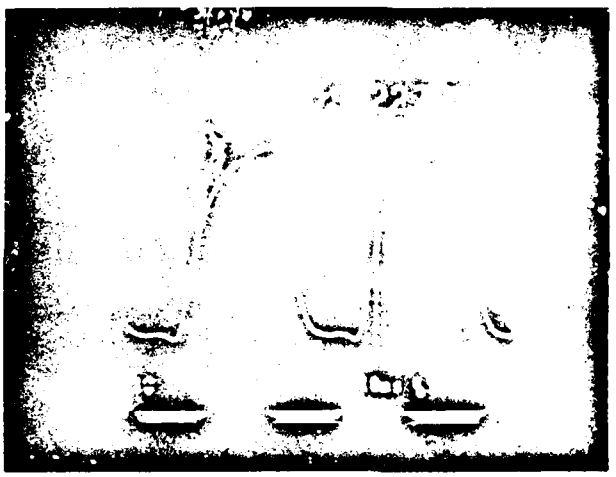


Figure 5.6: Experimental Results of Schmitt-trigger Oscillator

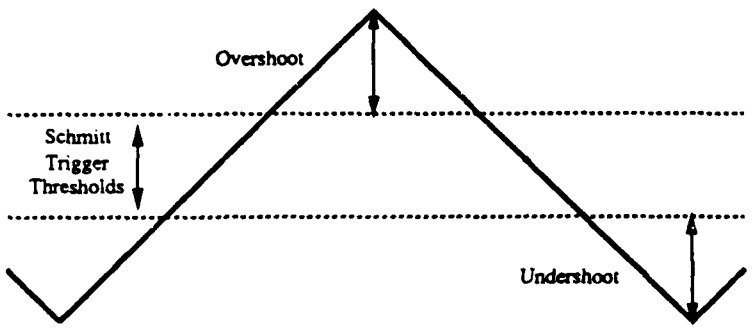


Figure 5.7: Overshoot Voltage on Internal Capacitor

the Schmitt-trigger oscillator, but with decreased performance due to the external test pins.

The goal of the divider circuit was to produce a 50% duty cycle square wave. Figure 5.8 shows the divider 50% duty cycle output regardless of input duty cycle. In the top photograph of Fig. 5.8, the input signal had a 20% duty cycle, and in the bottom photograph, the input signal had an 80% duty cycle. Both resulted in a 50% duty cycle output.

In Fig. 5.9 the divider was driven by the 22 MHz output signal of the Schmitt-trigger oscillator. The two photographs demonstrate the 50% duty cycle which the divider produced.

The transitions of the phase splitter are shown in Fig. 5.10. The transitions cross a volt below the midpoint of the supply rails, corresponding to a 3 ns delay.

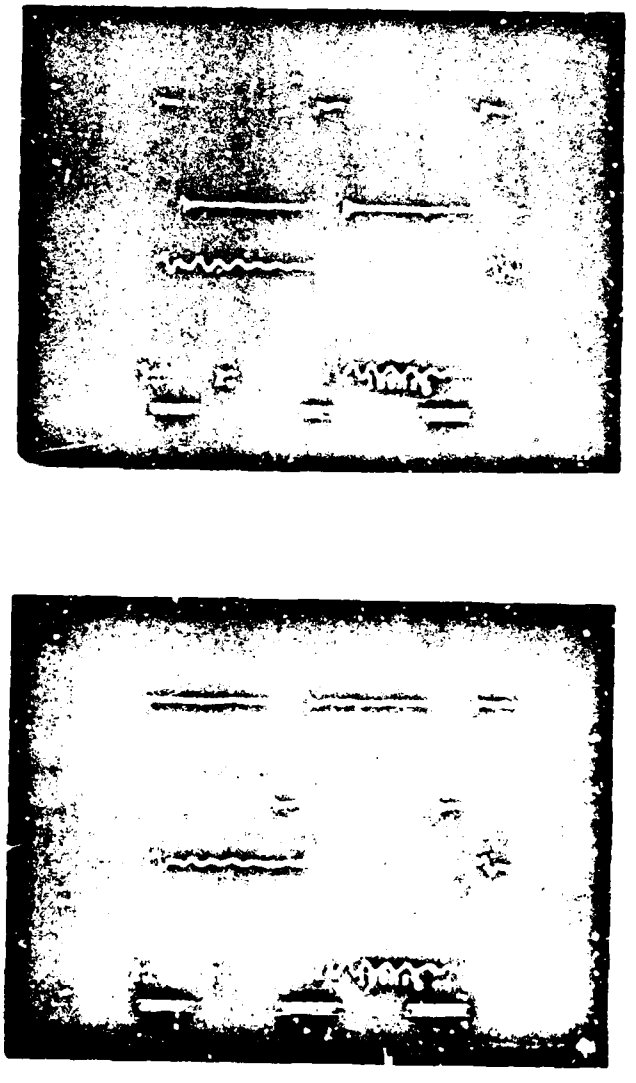


Figure 5.8: Experimental Divider Waveforms

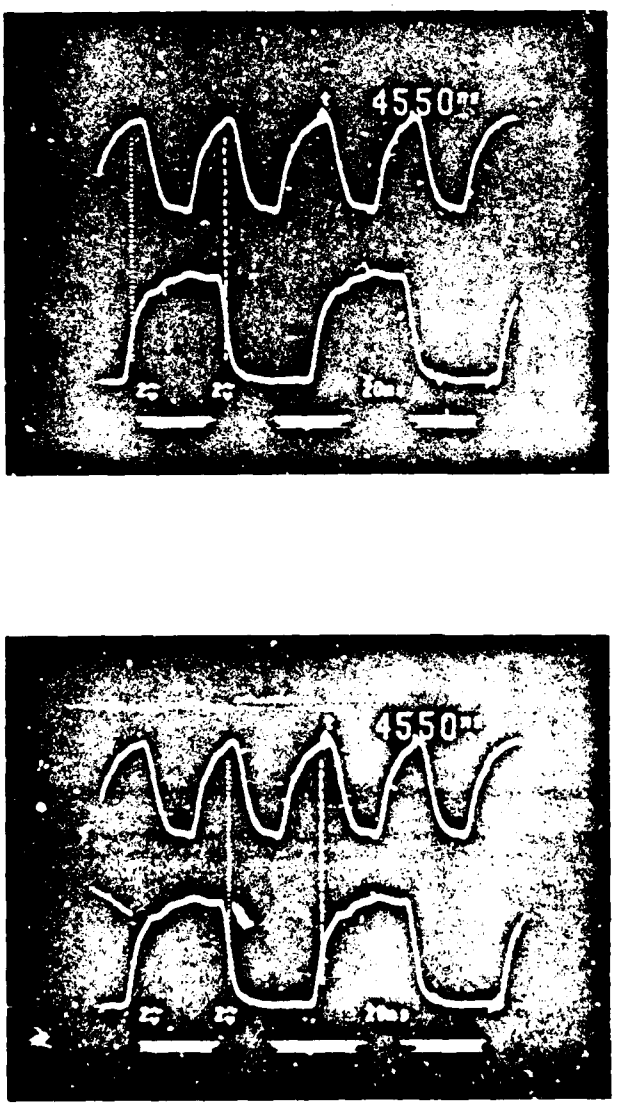


Figure 5.9: Experimental Divider Driven by Schmitt-trigger Oscillator

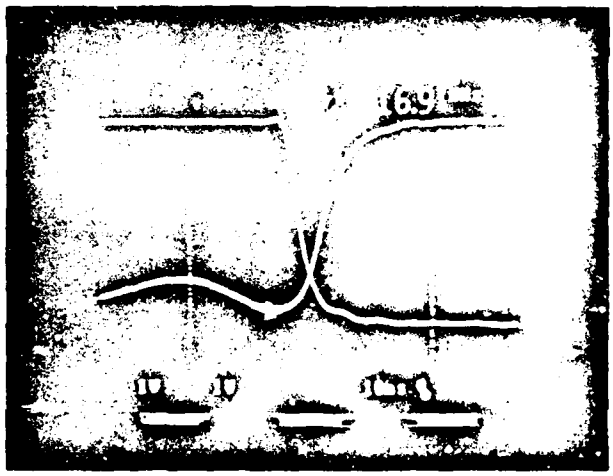


Figure 5.10: Experimental Phase Splitter Transitions

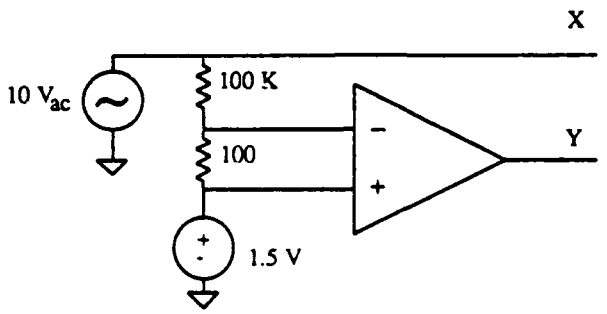


Figure 5.11: Circuit used to Test Open Loop Gain

5.3 Error Amplifier

The error amplifier consists of two pieces: the folded cascode operational amplifier and an analog inverter needed for startup conditions. The two pieces were fabricated separately to allow for independent testing.

5.3.1 Folded Cascode Operational Amplifier

The DC gain of the folded cascode operational amplifier was measured open loop, as shown in Fig. 5.11. The 10 volt input signal controlled the oscilloscope's x deflection and the op amp output controlled the y deflection. The DC gain of the op amp was then just the slope of the trace multiplied by 1000 due to the resistor divider. Figure 5.12 shows the experimental results. The open loop gain of the experimental folded cascode amplifier is

$$A_v = \frac{(1.92\ V)}{(10\ V)}(1000) = 192 \qquad (5.2)$$

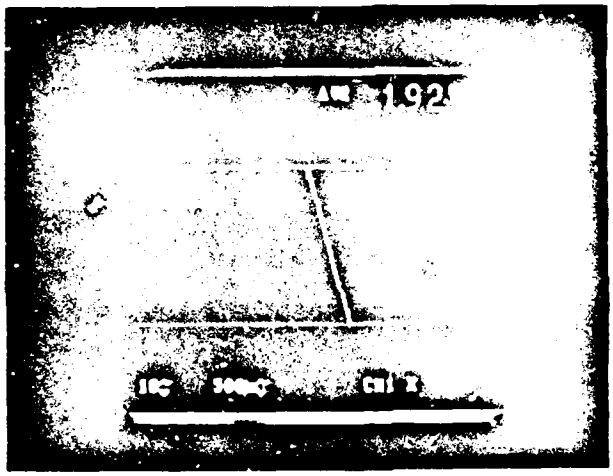


Figure 5.12: Experimental Results of DC Gain Measurements

The measured gain is a factor of ten smaller than predicted by hand calculations and simulations. This dramatic decrease in gain is caused by the failure of the improved cascode current source to properly bias the amplifier. Figure 5.13 shows the improved cascode current mirror that was used to bias the cascoded stage of the operational amplifier. This current mirror was used to improve the output swing of the amplifier. The improved cascode current source achieves the increased swing by sizing device M3 at 1/4 the W/L ratio of transistors M1,M2, and M4. In theory and in simulation, the proposed biasing scheme provides a V_{DS} of ΔV across both M5 and M6, as shown in Fig. 5.13. Thus, for a given drain current, both transistors are right on the edge of saturation as shown in Fig. 5.14. However, the slightest increase in the W/4L sizing of device M3 causes the lower device, M6, to enter the triode region. When the lower device enters the triode region, its output impedance decreases drastically. As can be seen from in Fig. 5.14, the slope of the I_D vs. V_{DS} curve sharply increases in the triode region, corresponding to a decreased output impedance.

In the folded cascode circuit shown in Fig. 5.15, the output impedance of the amplifier was derived assuming a high output impedance of the lower bias transistors, M3 and M4. Biasing M3 and M4 in the triode region effectively places a very low impedance in parallel with the high output impedance of the differential stage. The degraded gain is then

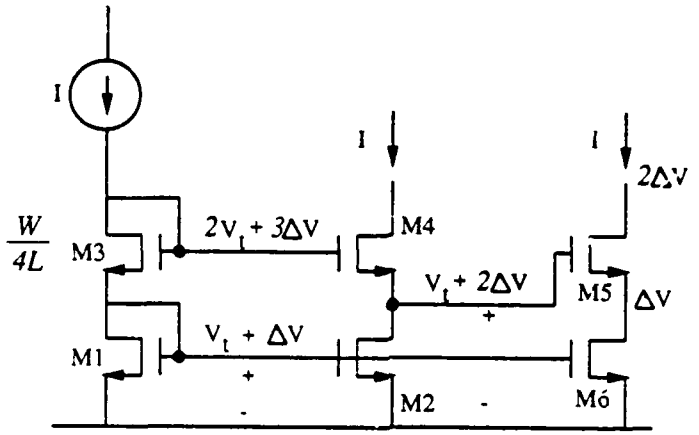


Figure 5.13: Improved Cascode Current Mirror

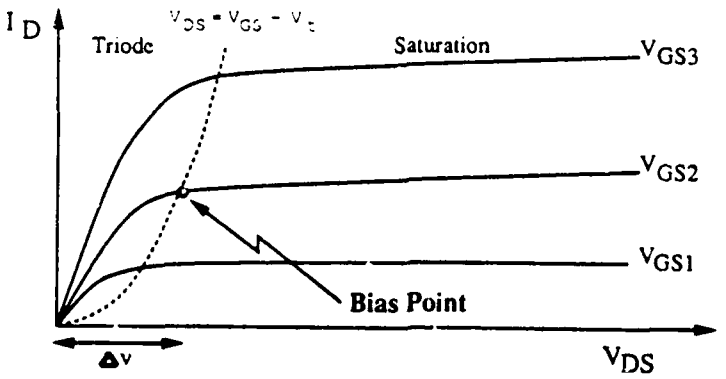


Figure 5.14: Biasing Point of Improved Cascode Current Mirror

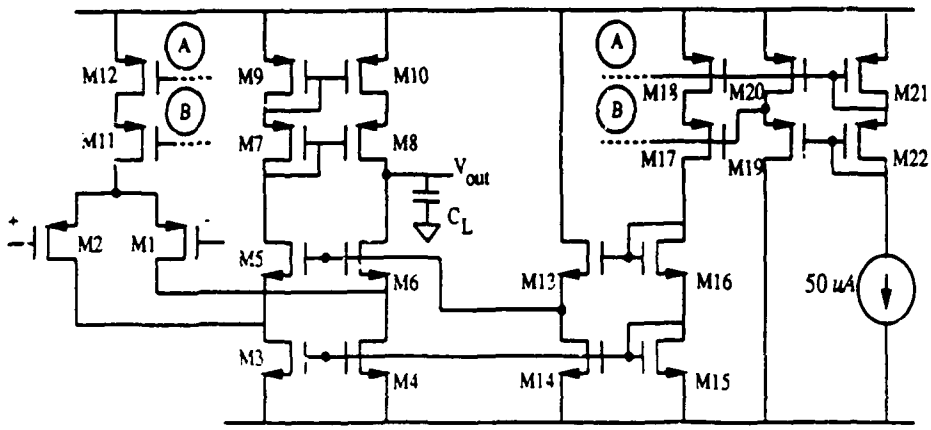


Figure 5.15: Folded Cascode Amplifier Circuit

$$A_v = g_{m_1} g_{m_6} r_{o_6} (r_{o_1} \,//\, R_{small}) \tag{5.3}$$

However, the improved cascode current mirror is still a viable bias network if precaution for non-ideality is taken. If transistor M3 of the Fig. 5.13 is sized to be W/5L or W/6L, saturation is assured with little sacrifice in output voltage swing. For instance, a W/6L ratio only reduces output swing to $2.5\Delta V$.

The decreased open loop gain of the amplifier also degrades its common mode rejection ratio and power supply rejection ratio. Common mode rejection ratio is defined as [11]

$$CMRR = \frac{A_D}{A_C} \tag{5.4}$$

	Expected	Measured
CMRR (at DC)	98 dB	75.56 dB
PSRR (at DC)	69 dB	46 dB

Table 5.1: Rejection Ratio Degradation Due to Decreased Differential Gain

where A_D is the differential gain and A_C is the common mode gain. Similarly, the power supply rejection ratio is defined as [11]

$$PSRR = \frac{A_D}{A_P} \tag{5.5}$$

where A_P is the gain at the output to a signal on the power supply rail. Since the differential gain, A_D, of the experimental folded cascode stage was a factor of ten less than expected, the CMRR and PSRR exhibited a corresponding factor of ten decrease. The experimental results are shown in Table 5.1.

5.3.2 Analog Inverter

As previously discussed, the amplifier output needs to be inverted in order to feed back a low signal to the primary side when the converter output was low. The analog inverter was first tested separately before attaching the operational amplifier. A 1 kHz, 200 mV sine wave was applied to the analog inverter. The experimental results showing the desired 180 degrees of phase shift are shown in Fig. 5.16. The top trace is the input signal, the bottom trace is the output signal. The maximum output swing of the inverter stage was 1 V_{p-p}, slightly less than the 1.5 volt simulated swing. The cause was a slightly lower bias voltage from the diode chain used to bias the inverter.

Figure 5.16: Input and Output Waveforms of Experimental Inverter

When connected to the folded cascode operational amplifier, the inverter-op amp pair exhibited a unity gain bandwidth of 4.93 MHz. This lower than expected bandwidth resulted from the capacitance added by splitting the two systems apart. The op amp vas compensated by adding a compensation capacitor to the output node. Since the amplifier and the inverter were fabricated separately, connecting them required connecting two external pins on the IC. The output pin of the operational amplifier and the input pin of the inverter, with their associated bonding pads, added approximately 20 pF to the compensation capacitor. The added capacitance pushed the dominant pole lower in frequency and decreased the bandwidth. Connecting the amplifier and inverter on chip would restore the bandwidth of the system.

In addition, all of the offsets through the inverter were not exactly canceled by sizing, as was simulated. The input offset voltage of the amplifier-inverter pair was 4.64 mV. The offsets produced by the inverter can be attributed to the differences in threshold voltages between the models used for simulation and the fabricated devices. Table 5.2 summarizes the test results of the error amplifier.

5.4 Modulator

A layout mask error prevented experimental testing of the modulator. The defect occurred over the active area of a transistor such that any FIB repair would destroy the device. At the the time of this writing, an updated edition

Parameter	Test Condition		units
Input Offset Voltage	$V_{cm} = 1.5V$	4.64	mV
Input Bias Current	$V_{cm} = 1.5V$	0	μA
Input Offset Current	$V_{cm} = 1.5V$	0	μA
Small Signal Open Loop Gain		45.66	dB
CMRR	V_{cm} 1 - 3.5 V	75.56	dB
PSRR	DC	46	dB
Output Swing		1.0	V
Max Sink Current		500	μA
Max Source Current		5	mA
Unity Gain Bandwidth		4.93	MHz

Table 5.2: Error Amplifier Test Results

of the secondary-side isolated feedback controller integrated circuit is being prepared for submission to MOSIS. The upgraded layout contained subcell design improvements and connected the individual elements of the circuit.

Chapter 6

Conclusion

This thesis described the development of a CMOS secondary side feedback control integrated circuit. The main functional components of the circuit were fabricated through the MOSIS program and tested independently.

The bandgap reference circuit provided a voltage reference that was stable to within ± 0.3% over the commercial 0-70°C temperature range. When the temperature was increased to include the upper 125°C limit of the military temperature range, the circuit was still stable to ± 1.1%. Given the uncertainty of MOSIS process parameters, the circuits required trimming to achieve the 0.3% accuracy. The resistor trimming technique was intended only for evaluation of the prototype. When the design is targeted for a specific process, the trimming process could presumably be eliminated.

The oscillator subsection was compiled from a modified library of existing subcells of power supply control circuitry. The circuits were scaled down to the two micron process and adapted to function with a 5 volt power

supply. All of the subcells demonstrated proper circuit operation, although each exhibited an explainable performance degradation due to the added parasitics involved with bringing internal signals off chip for measurement. The implementation of previously designed CMOS control circuitry in an upgraded technology demonstrated the versatility of the CMOS technology for power supply control. Due to the scalable nature of CMOS, existing libraries of subcells remain viable as technologies improve. Utilizing these libraries of CMOS subcells facilitates rapid implementation of application-specific control circuitry.

The error amplifier demonstrated a disappointing factor of ten decrease in gain from that predicted by simulation. The cause was traced to a design error in the improved cascode current source used to bias the amplifier. Resizing one device would eliminate the biasing problem and restore performance.

The implementation of the feedback controller IC also involved an investigation into the use of a Focused Ion Beam for integrated circuit repair. Experiments with samples of the feedback controller IC demonstrated the feasibility of both connecting and severing aluminum lines with the Focused Ion Beam. Unfortunately, the modulator subcell layout contained an error that was unrepairable with the FIB, rendering the circuit inoperable.

Opportunities for future work include combining all of the subcells presented in this thesis into a monolithic integrated circuit and testing the con-

troller in a prototype power converter. An additional application of CMOS control circuitry includes integrating the primary side control. In current point-of-load converters, the demodulation of the amplitude modulated feedback signal is accomplished with a peak detection circuit implemented with discrete components. Integration of the demodulator circuit with the primary side control circuitry would allow further reduction of converter size.

Appendix A

Microphotographs of Integrated Circuits

Figure A.1 is a microphotograph of the integrated circuit fabricated to test the functional blocks of the feedback controller. Starting from the lower left-hand corner and proceeding counter-clockwise, the circuit blocks are: the Schmitt-trigger oscillator, the divider, the phase splitter, the error amplifier, the modulator, the error amplifier inverter, the bandgap operational amplifier, and two complete bandgap reference circuits.

Figure A.2 is a microphotograph of the integrated circuit fabricated to test the bandgap reference circuit. The chip contains six bandgap circuits, three along the left side, three along the right side, as well as individual resistors and bipolar transistors.

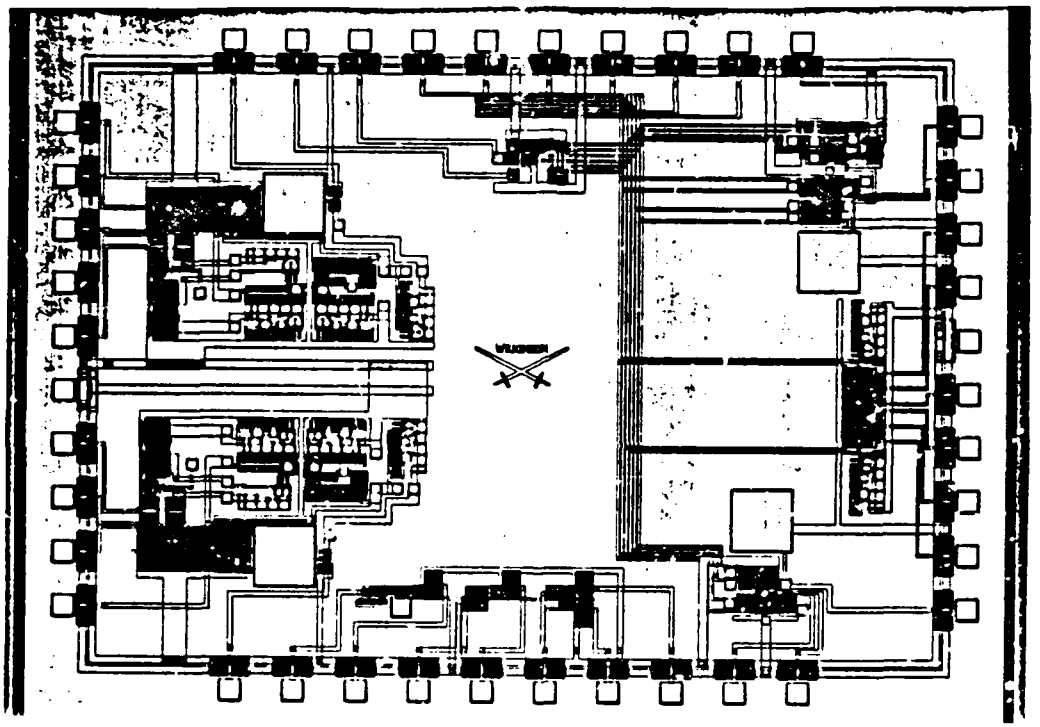


Figure A.1: Fabrication of Separate Functional Blocks

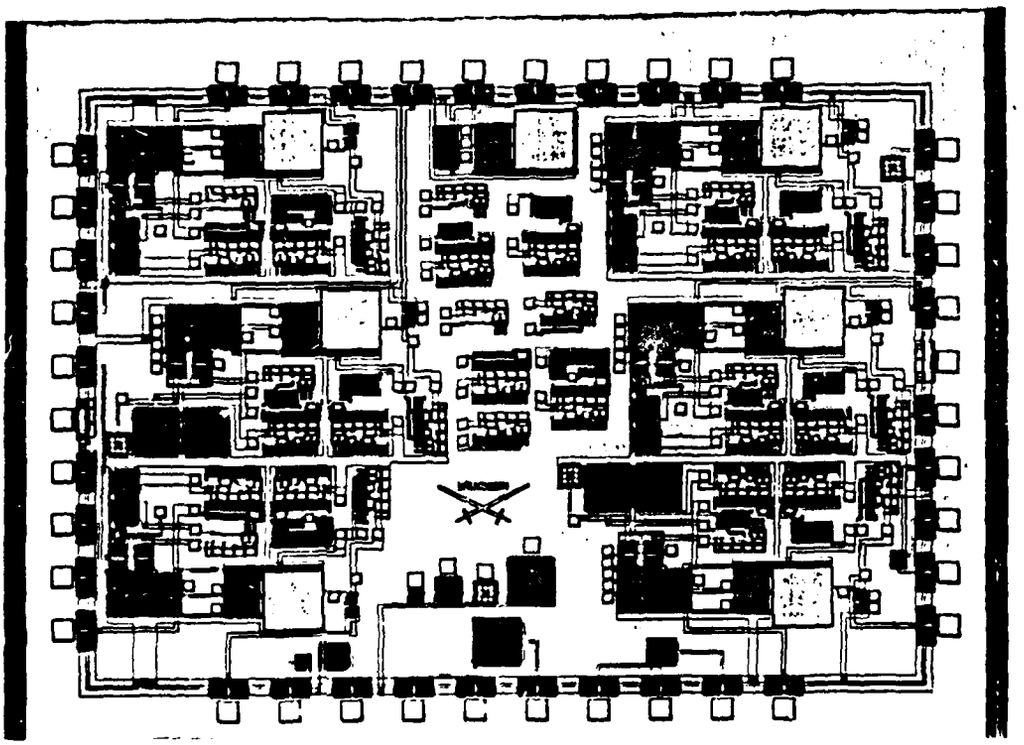


Figure A.2: Fabrication of Bandgap Circuits

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